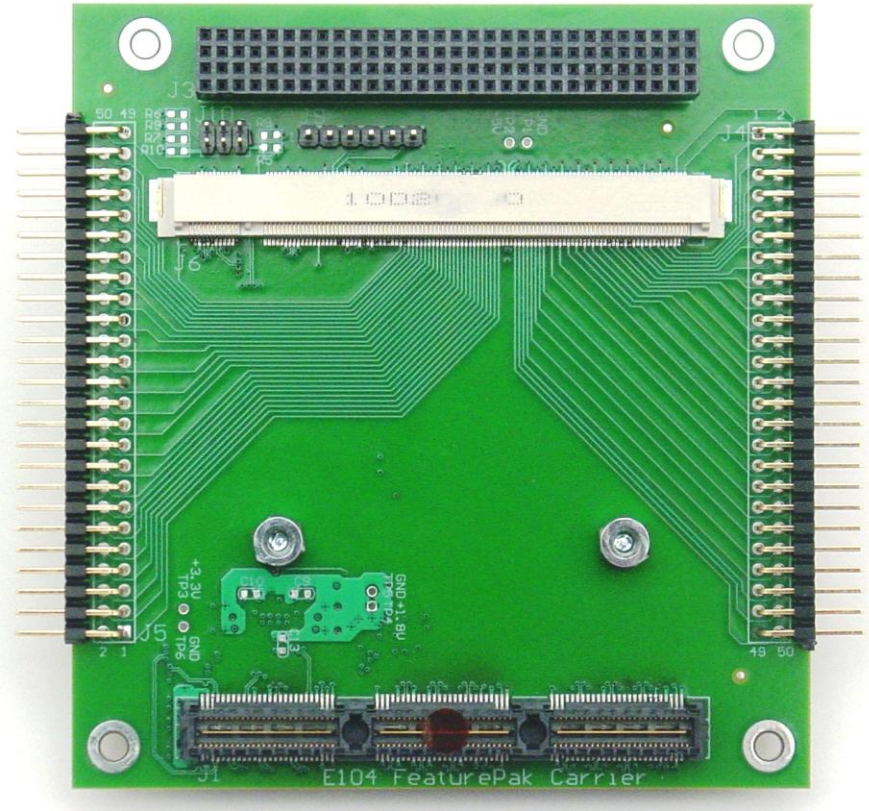
PCIe/104 / FEATUREPAK ADAPTER MODULE

User Manual

Revision A.01 November 2013



Revision	Date	Comment
A.00	4/25/11	Initial Release
A.01	11/18/12	Added FeaturePak pinout Appendix

FOR TECHNICAL SUPPORT PLEASE CONTACT:

support@diamondsystems.com

Diamond Systems Corporation
555 Ellis Street
Mountain View, CA 94043 USA
Tel 1-650-810-2500
Fax 1-650-810-2525
www.diamondsystems.com

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IMPORTANT SAFE-HANDLING INFORMATION

WARNING: ESD-Sensitive Electronic Equipment!

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

Aurora contains numerous I/O connectors that connect to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

ESD damage – This type of damage is almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board simply stops working, because some component becomes defective. Usually the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage – On some boards we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards – Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply. In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

Bent connector pins – This type of problem is often only a cosmetic issue and is easily fixed by bending the pins back to their proper shape one at a time with needle-nose pliers. This situation can occur when pulling a ribbon cable off of a pin header. Note: If the pins are bent too severely, bending them back can cause them to weaken unacceptably or even break, and the connector must be replaced.

1. DESCRIPTION

The E104/FP Adapter Module allows the use of FeaturePak™ I/O expansion modules in systems that provide PCIe/104™ expansion stack locations.

This board is an ISM-format carrier module that provides a socket and host connectivity for a FeaturePak module using one x1 PCI Express link on a PCIe/104 connector. It does not provide for all possible host connections to the FeaturePak module, because to do so would consume excessive resources on the connector.

1.1 Features

Key E104/FP Adapter features include:

1.1.1 PCI Express

- Provides one x1 link of PCI Express from the PCIe/104 connector to the FeaturePak module
- Provides lane shifting for remaining PCI Express links on the PCIe/104 connector
- Supports both top and bottom stacking configurations with jumper-selected link selection

1.1.2 FeaturePak

- Provides one socket for a FeaturePak I/O module
- Provides 2 dual-row right angle 50-pin connectors with .1" pin spacing for cable connection to the FeaturePak I/O groups
- Provides FeaturePak slot ID selection with a jumper block and optional hard-wired zero-ohm resistors

1.1.3 Miscellaneous

- Includes PCI-104 connector as an assembly option for pass-through of the PCI-104 bus

1.1.4 Omitted Features

- The module provides only one x1 PCI Express link to the FeaturePak module, although the FeaturePak specification allows up to two x1 links.
- The module does not provide a USB connection to the FeaturePak module, although the FeaturePak specification allows for up to one link.
- The module does not provide a means to connect to the FeaturePak module using its TTL serial interface option.
- The module does not provide for the Reset Out function defined by the FeaturePak specification, because no such feature exists on the PCIe/104 connector.
- The module does not provide for the FeaturePak Present output from the FeaturePak module, because no such feature exists on the PCIe/104 connector.

1.1.5 Environmental / Mechanical

- ISM format board, 3.55"W x 3.775"H
- PCIe/104 stackthrough configuration
- PCI Express x1 host interface
- -40°C to +85°C operating temperature

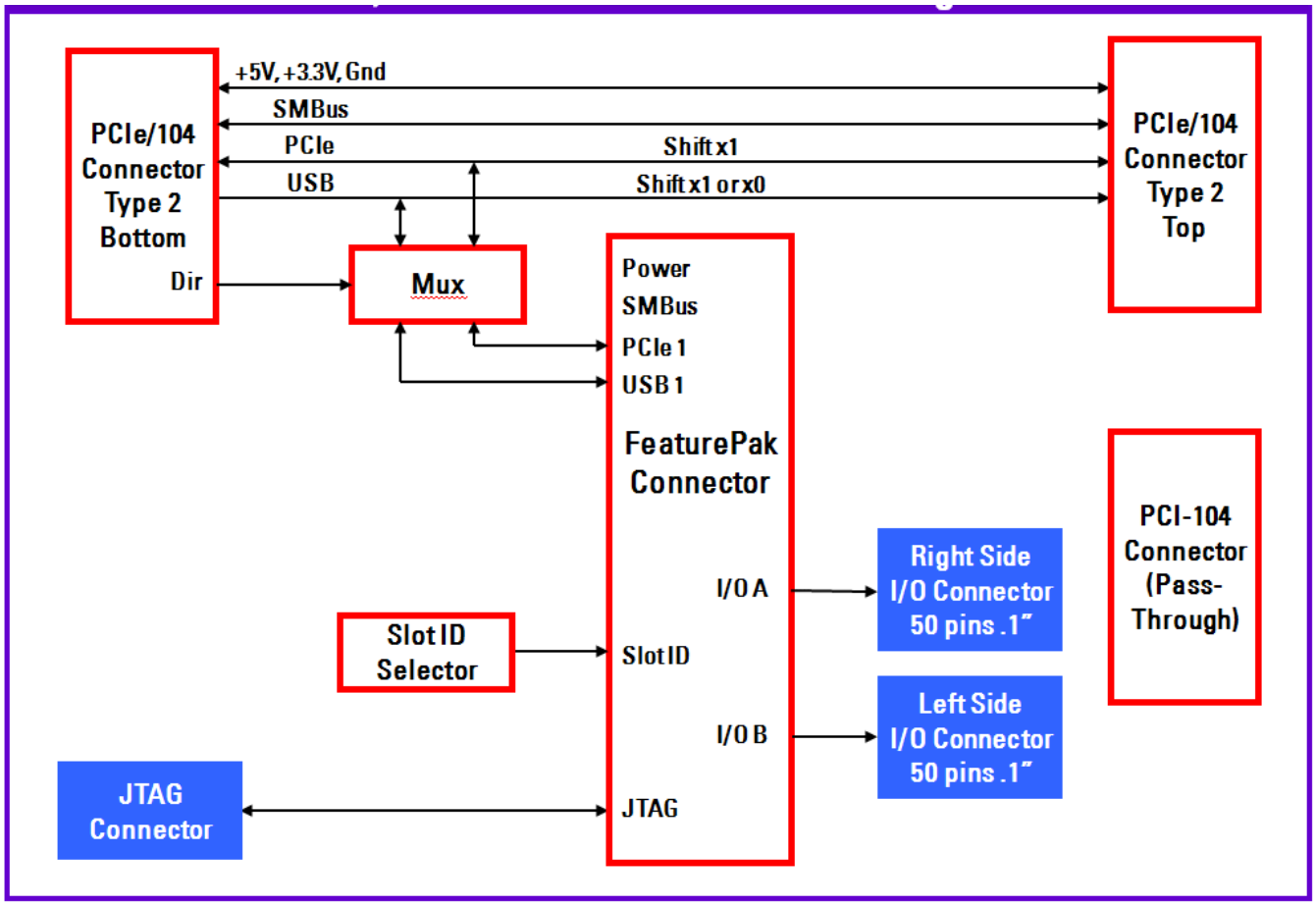
For more information about the FeaturePak specification, please refer to the FeaturePak website at http://www.featurepak.org. For more information on the PCIe/104 standard, please refer to www.pc104.org.

1.2 FeaturePak Resources

The E104/FP Adapter uses the FeaturePak resources indicated in the table below.

FeaturePak™ Socket Resources	
Company: Diamond Systems Corp.	
Product: E104/FP Adapter	
Host Interface Resources Supported	
PCIe x1 links	1 (1)
USB channels	1 USB 2.0 (1)
Serial port	√
SMBus	√
PCIe Reset	√
Sys Reset	–
JTAG	√
+3.3V	√
+5V	√
+12V	opt
Notes: (1) Depends on host SUMIT stack. www.featurepak.org/label	

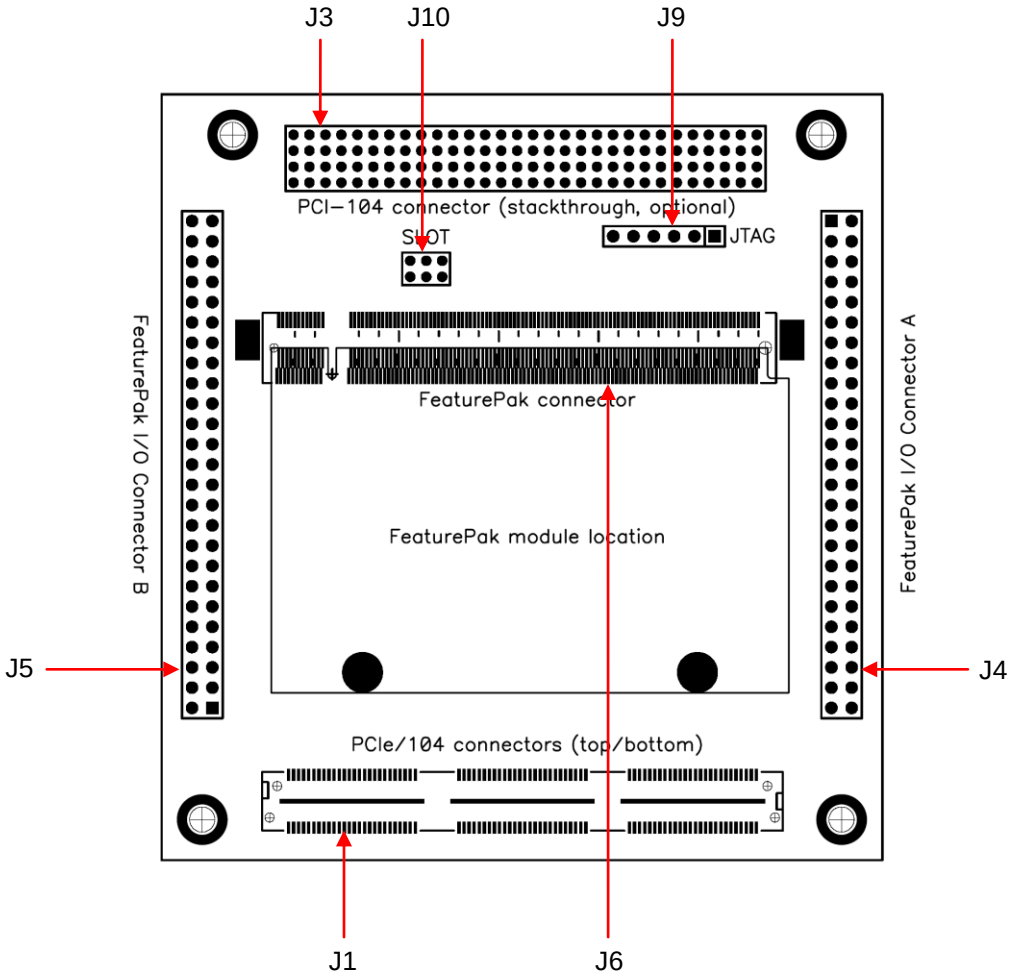
2. BLOCK DIAGRAM



3. MECHANICAL DRAWING

The module conforms to the PCIe/104 mechanical format. FeaturePak I/O group A is brought out to the right side I/O connector, and I/O group B is brought out to the left side.

All I/O connectors are located on the board so that there is sufficient room to install all connectors without interference from any other connector or mounting hole. There are two mounting holes to secure the FeaturePak module to the E104/FP Adapter Module.



4. FUNCTIONAL DESCRIPTION

The board connects a PCI Express x1 link from the PCIe/104 connector to the first PCIe link on on the FeaturePak connector. It provides a high-speed switch rated for PCI Express for selection of either the first or last x1 link, depending on whether the module will be stacked above or below the SBC. Link selection is automatic based on the voltage level of the DIR pin on the PCIe/104 connector.

The board offers the option to switch a USB link to the FeaturePak connector by means of resistor configuration. In the USB configuration, the first and second USB ports on the PCIe/104 connector are also routed through the switch to the FeaturePak first USB link, and the links are shifted between the top and bottom PCIe/104 connectors. In the non-USB configuration, the USB links are routed straight through between the top and bottom PCIe/104 connectors, and no link is routed to the FeaturePak connector.

FeaturePak I/O is provided with two 50-pin connectors on the left and right sides of the board. These connectors work with standard .050" pitch ribbon cables. Connector A is on the right side of the board, and connector B is on the left side.

A JTAG connector is provided to enable access to the JTAG signals on the FeaturePak connector. This JTAG connector may be used to reprogram FPGA or other logic on the FeaturePak module.

A 2x3 2mm pitch jumper block is provided to select the FeaturePak slot ID. This ID may be set for any number between 1 and 6; numbers 0 and 7 are reserved. A jumper installed means a 1, and an open position means a 0. Each jumper may be replaced by a discrete zero-ohm resistor soldered on the board to provide a hardwired configuration.

The PCI-104 connector footprint is included on the module for optional inclusion to support pass-through of the PCI-104 bus to another module in the stack. This connector is not used by any circuitry on the module, and its power and ground pins are not connected on the board.

5. CONNECTORS AND JUMPERS

All of the following connectors are on the top side of the board. Connector and pinout information is provided in the following sections.

5.1 FeaturePak Connector, J6

The E104/FP Adapter Module typically comes with a FeaturePak module installed in the FeaturePak connector. The inserted FeaturePak module defines the signals that are provided to the user. The FeaturePak connector, J6, is a compact MXM connector that provides 230 contacts organized into two rows of 115 contacts, with 0.5mm pitch. The connector is rated for 2.5Gbps operation, making it suitable for PCI Express, USB, and other high speed signals. It contains an alignment pin to ensure proper orientation of the FeaturePak module during insertion. The alignment pin is the primary reference point for the relative position of the module and the connector.

FeaturePak Connector Pinout

+3.3V	1	2	+12V
+3.3V	3	4	PS-Current
Ground	5	6	Ground
PCIe-TX1+	7	8	PCIe-RX1+
PCIe-TX1-	9	10	PCIe-RX1-
Ground	11	12	Ground
PCIe-CLK1+	13	14	PCIe-CLK2+
PCIe-CLK1-	15	16	PCIe-CLK2-
Ground	17	18	Ground
PCIe-TX2+	19	20	PCIe-RX2+
PCIe-TX2-	21	22	PCIe-RX2-
Ground	23	24	Ground
PCIe-Reset-	25	26	LPC-CLK
LPC-SERIRQ	27	28	LPC-DRQ
LPC-Reset-	29	30	LPC-Frame-
LPC-AD3	31	32	LPC-AD2
LPC-AD1	33	34	LPC-AD0
Ground	35	36	Ground
USB-Ch1+	37	38	USB-Ch2+
USB-Ch1-	39	40	USB-Ch2-
Ground	41	42	Ground
+3.3V	43	44	USB-OC1/2-
+3.3V	45	46	Serial-RX1
Serial-TX1	47	48	Serial-CTS1
Serial-RTS1	49	50	SMBclk
SMBalert#	51	52	SMBdata
Slot ID 2	53	54	Slot ID 1
Slot ID 0	55	56	Present-
JTAG-TDI	57	58	JTAG-TDO
JTAG-CLK	59	60	JTAG-TMS
Sys-Reset-	61	62	Reserved
+3.3V	63	64	Ground
+3.3V	65	66	Ground
Reserved	67	68	Reserved
Reserved	69	70	Reserved
+3.3V	71	72	Ground
Reserved	73	74	Reserved
Reserved	75	76	Reserved
+3.3V	77	78	Ground
Reserved	79	80	Reserved
Reserved	81	82	Reserved
Reserved	83	84	Reserved
Reserved	85	86	Reserved

+5V	87	88	Ground
+5V	89	90	Ground
I/OB-50	91	92	I/OB-49
I/OB-48	93	94	I/OB-47
I/OB-46	95	96	I/OB-45
I/OB-44	97	98	I/OB-43
I/OB-42	99	100	I/OB-41
I/OB-40	101	102	I/OB-39
I/OB-38	103	104	I/OB-37
I/OB-36	105	106	I/OB-35
I/OB-34	107	108	I/OB-33
I/OB-32	109	110	I/OB-31
I/OB-30	111	112	I/OB-29
I/OB-28	113	114	I/OB-27
I/OB-26	115	116	I/OB-25
I/OB-24	117	118	I/OB-23
I/OB-22	119	120	I/OB-21
I/OB-20	121	122	I/OB-19
I/OB-18	123	124	I/OB-17
I/OB-16	125	126	I/OB-15
I/OB-14	127	128	I/OB-13
I/OB-12	129	130	I/OB-11
I/OB-10	131	132	I/OB-9
I/OB-8	133	134	I/OB-7
I/OB-6	135	136	I/OB-5
I/OB-4	137	138	I/OB-3
I/OB-2	139	140	I/OB-1

+5V	141	142	Ground
+5V	143	144	Ground
+5V	145	146	Ground
I/OA-50	147	148	I/OA-49
I/OA-48	149	150	I/OA-47
I/OA-46	151	152	I/OA-45
I/OA-44	153	154	I/OA-43
I/OA-42	155	156	I/OA-41
I/OA-40	157	158	I/OA-39
I/OA-38	159	160	I/OA-37
I/OA-36	161	162	I/OA-35
(NC)	163	164	(NC)
I/OA-34	165	166	I/OA-33
(NC)	167	168	(NC)
I/OA-32	169	170	I/OA-31
(NC)	171	172	(NC)
I/OA-30	173	174	I/OA-29
(NC)	175	176	(NC)
I/OA-28	177	178	I/OA-27
(NC)	179	180	(NC)
I/OA-26	181	182	I/OA-25
(NC)	183	184	(NC)
I/OA-24	185	186	I/OA-23
(NC)	187	188	(NC)
I/OA-22	189	190	I/OA-21
(NC)	191	192	(NC)
I/OA-20	193	194	I/OA-19
(NC)	195	196	(NC)
I/OA-18	197	198	I/OA-17
(NC)	199	200	(NC)
I/OA-16	201	202	I/OA-15
(NC)	203	204	(NC)
I/OA-14	205	206	I/OA-13
(NC)	207	208	(NC)
I/OA-12	209	210	I/OA-11
(NC)	211	212	(NC)
I/OA-10	213	214	I/OA-9
(NC)	215	216	(NC)
I/OA-8	217	218	I/OA-7
(NC)	219	220	(NC)
I/OA-6	221	222	I/OA-5
(NC)	223	224	(NC)
I/OA-4	225	226	I/OA-3
(NC)	227	228	(NC)
I/OA-2	229	230	I/OA-1

5.2 I/O Connectors, J4 and J5

The FeaturePak I/O signals are brought out to two connectors: Port A and Port B. Port A is labeled as J4 on the PBC, and Port B is labeled as J5. Each port I/O connector is a .1" dual row 50-pin male right angle connector. The pins from the FeaturePak connector are brought out to the Port A and Port B connectors as defined in the following table.

FeaturePak Connector Pin	Port A Pin		FeaturePak Connector Pin
230	**1**	**2**	229
226	**3**	**4**	225
222	**5**	**6**	221
218	**7**	**8**	217
214	**9**	**10**	213
210	**11**	**12**	209
206	**13**	**14**	205
202	**15**	**16**	201
198	**17**	**18**	197
194	**19**	**20**	193
190	**21**	**22**	189
186	**23**	**24**	185
182	**25**	**26**	181
178	**27**	**28**	177
174	**29**	**30**	173
170	**31**	**32**	169
166	**33**	**34**	165
162	**35**	**36**	161
160	**37**	**38**	159
158	**39**	**40**	157
156	**41**	**42**	155
154	**43**	**44**	153
152	**45**	**46**	151
150	**47**	**48**	149
148	**49**	**50**	147

FeaturePak Connector Pin	Port B Pin		FeaturePak Connector Pin
140	**1**	**2**	139
138	**3**	**4**	137
136	**5**	**6**	135
134	**7**	**8**	133
132	**9**	**10**	131
130	**11**	**12**	129
128	**13**	**14**	127
126	**15**	**16**	125
124	**17**	**18**	123
122	**19**	**20**	121
120	**21**	**22**	119
118	**23**	**24**	117
116	**25**	**26**	115
114	**27**	**28**	113
112	**29**	**30**	111
110	**31**	**32**	109
108	**33**	**34**	107
106	**35**	**36**	105
104	**37**	**38**	103
102	**39**	**40**	101
100	**41**	**42**	99
98	**43**	**44**	97
96	**45**	**46**	95
94	**47**	**48**	93
92	**49**	**50**	91

5.3 JTAG Connector, J9

The JTAG connector, J9, passes the defined signals to their equivalent on the FeaturePak connector, enabling an installed FeaturePak module to be reprogrammed. This is a standard .1" 6-pin single row straight pin header connector with gold flash plating.

+3.3V	1
Ground	2
JTAG-CLK	3
JTAG-TDO	4
JTAG-TD1	5
JTAG-TMS	6

5.4 PCIe/104 Connector, J1

The PCIe/104 bus is essentially identical to the PCI Express Bus except for the physical design. In the pinout figures below, the tops correspond to the left edge of the connector when the board is viewed from the primary side (side with the female end of the PCIe/104 connector) and the board is oriented so that the PCIe/104 connectors are along the bottom edge of the board.

For more information on the PCIe/104 specification, visit the PC/104 Embedded Consortium website, at http://www.pc104.org.

View from Top of Board

Reserved	1	2	PE_RST#	Reserved	53	54	PEG_ENA#
3.3V	3	4	3.3V	Ground	55	56	Ground
Reserved	5	6	Reserved	PEx16_0T(8)p	57	58	PEx16_0T(0)p
Reserved	7	8	Reserved	PEx16_0T(8)n	59	60	PEx16_0T(0)n
Ground	9	10	Ground	Ground	61	62	Ground
PEx1_1Tp	11	12	PEx1_0Tp	PEx16_0T(9)p	63	64	PEx16_0T(1)p
PEx1_1Tn	13	14	PEx1_0Tn	PEx16_0T(9)n	65	66	PEx16_0T(1)n
Ground	15	16	Ground	Ground	67	68	Ground
PEx1_2Tp	17	18	PEx1_3Tp	PEx16_0T(10)p	69	70	PEx16_0T(2)p
PEx1_2Tn	19	20	PEx1_3Tn	PEx16_0T(10)n	71	72	PEx16_0T(2)n
Ground	21	22	Ground	Ground	73	74	Ground
PEx1_1Rp	23	24	PEx1_0Rp	PEx16_0T(11)p	75	76	PEx16_0T(3)p
PEx1_1Rn	25	26	PEx1_0Rn	PEx16_0T(11)n	77	78	PEx16_0T(3)n
Ground	27	28	Ground	Ground	79	80	Ground
PEx1_2Rp	29	30	PEx1_3Rp	PEx16_0T(12)p	81	82	PEx16_0T(4)p
PEx1_2Rn	31	32	PEx1_3Rn	PEx16_0T(12)n	83	84	PEx16_0T(4)n
Ground	33	34	Ground	Ground	85	86	Ground
PEx1_1Clkp	35	36	PEx1_0Clkp	PEx16_0T(13)p	87	88	PEx16_0T(5)p
PEx1_1Clkn	37	38	PEx1_0Clkn	PEx16_0T(13)n	89	90	PEx16_0T(5)n
5V_Always	39	40	5V_Always	Ground	91	92	Ground
PEx1_2Clkp	41	42	PEx1_3Clkp	PEx16_0T(14)p	93	94	PEx16_0T(6)p
PEx1_2Clkn	43	44	PEx1_3Clkn	PEx16_0T(14)n	95	96	PEx16_0T(6)n
CPU_DIR	45	46	PWRGOOD	Ground	97	98	Ground
SMB_DAT	47	48	PEx16_x8_x4Clkp	PEx16_0T(15)p	99	100	PEx16_0T(7)p
SMB-CLK	49	50	PEx16_x8_x4_Clkn	PEx16_0T(15)n	101	102	PEx16_0T(7)n
SMB_Alert	51	52	PSON#	Ground	103	104	Ground

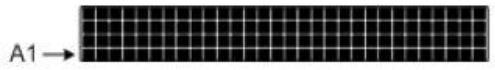
View from Top of Board

SDVO_DAT (PENA#)	105	106	SDVO_CLK
Ground	107	108	Ground
PEx16_0R(8)p	109	110	PEx16_0R(0)p
PEx16_0R(8)n	111	112	PEx16_0R(0)n
Ground	113	114	Ground
PEx16_0R(9)p	115	116	PEx16_0R(1)p
PEx16_0R(9)n	117	118	PEx16_0R(1)n
Ground	119	120	Ground
PEx16_0R(10)p	121	122	PEx16_0R(2)p
PEx16_0R(10)n	123	124	PEx16_0R(2)n
Ground	125	126	Ground
PEx16_0R(11)p	127	128	PEx16_0R(3)p
PEx16_0R(11)n	129	130	PEx16_0R(3)n
Ground	131	132	Ground
PEx16_0R(12)p	133	134	PEx16_0R(4)p
PEx16_0R(12)n	135	136	PEx16_0R(4)n
Ground	137	138	Ground
PEx16_0R(13)p	139	140	PEx16_0R(5)p
PEx16_0R(13)n	141	142	PEx16_0R(5)n
Ground	143	144	Ground
PEx16_0R(14)p	145	146	PEx16_0R(6)p
PEx16_0R(14)n	147	148	PEx16_0R(6)n
Ground	149	150	Ground
PEx16_0R(15)p	151	152	PEx16_0R(7)p
PEx16_0R(15)n	153	154	PEx16_0R(7)n
Ground	155	156	Ground

5.5 PCI-104 Connector, J3

The PCI-104 bus is essentially identical to the PCI Bus except for the physical design. A single pin and socket connector is specified for the bus signals. A 120-pin header, J3, arranged as four 30-pin rows incorporates a full 32-bit, 33MHz PCI Bus. The additional pins on the PC/104-*Plus* connectors are used as ground or key pins. The female sockets on the top of the board enable stacking another PC/104-*Plus* board on top of the E104/FP Adapter Module. The E104/FP Adapter Module cannot be configured as a PCI bus master.

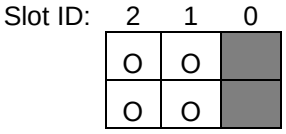
In the connector J3 pinout table, below, the top corresponds to the left edge of the connector when the board is viewed from the primary side (the side with the female end of the PC/104-*Plus* connector), and the board is oriented so that the PC/104 connectors are along the bottom edge of the board and the PC/104-*Plus* connector is in the top of the E104/FP Adapter Module.



Pin #	A	B	C	D
1	GND/5.0V KEY	Reserved	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	Reserved	PAR
10	GND	PERR*	+3.3V	Reserved
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DESEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	~REQ3	~GNT3	GND/3.3V KEY

5.6 Slot ID Selector Jumper Block, J10

The Slot ID Selector jumper block, J10, determines the slot ID of the board. The slot ID bits are identified on the board as Slot ID 2, 1, or 0. The three slot ID bits are pulled up or down through jumpers as follows: '0' = ground, '1' = +3.3V. The default Slot ID is 001 as shown in the table below.



6. APPENDIX A

Appendix A shows the pinouts for the PCIe/104 / FeaturePak Adapter Modules when used with Diamond Systems' FeaturePak modules; the FP-DAQ1616 and the FP-GPIO96.

6.1 FP-DAQ1616 Pinout

6.1.1 Port A: Analog I/O Signals

FeaturePak connector pin no.		Port A pin number			FeaturePak connector pin no.
230	Vin 0/0+	1	2	Vin 8/0-	229
226	Vin 1/1+	3	4	Vin 9/1-	225
222	Vin 2/2+	5	6	Vin 10/2-	221
218	Vin 3/3+	7	8	Vin 11/3-	217
214	Vin 4/4+	9	10	Vin 12/4-	213
210	Vin 5/5+	11	12	Vin 13/5-	209
206	Vin 6/6+	13	14	Vin 14/6-	205
202	Vin 7/7+	15	16	Vin 15/7-	201
198	Aground (Vin)	17	18	Aground (Vin)	197
194	Vout 0	19	20	Vout 8	193
190	Vout 1	21	22	Vout 9	189
186	Vout 2	23	24	Vout 10	185
182	Vout 3	25	26	Vout 11	181
178	Vout 4	27	28	Vout 12	177
174	Vout 5	29	30	Vout 13	173
170	Vout 6	31	32	Vout 14	169
166	Vout 7	33	34	Vout 15	165
162	Aground (Vout)	35	36	Aground (Vout)	161
160	ADTrig	37	38	Ctr0Clk	159
158	Ctr1Clk	39	40	Ctr1Out	157
156	Aux0	41	42	Aux1	155
154	Aux2	43	44	Aux3	153
152	ADGate / Aux4	45	46	Aux5 / Ctr1Gate	151
150	WDTOut / Aux6	47	48	Aux7 / WDTIn	149
148	+3.3V	49	50	Dground	147

Signal Name	Definition
Vin 7/7+ ~ Vin 0/0+	Analog input channels 7 – 0 in single-ended mode; High side of input channels 7 – 0 in differential mode
Vin 15/7- ~ Vin 8/0-	Analog input channels 15 – 8 in both single-ended mode; Low side of input channels 7 – 0 in differential mode
Vout 0-15	Analog output channels 0 – 15
Aground (Vout), (Vin)	Analog ground; used for analog signals only Vout pin is for the analog outputs; Vin pin is for the analog inputs
Dground	Digital ground reference for digital input signals
AD Gate	Enables A/D sampling when high or open, disables when pulled low
AD Trig	External A/D trigger or clock input
Ctr0Clk, Ctr1Clk	Counter 0/1 optional external clock inputs

Ctr1Out	Counter 1 output signal
AUX0-7	Auxiliary digital I/O port; bit direction programmable; Line 4-7 have auxiliary functions for A/D gating, counter gating, and watchdog timer.

6.1.2 Port B: Digital I/O Signals

FeaturePak connector pin no.		Port B pin number			FeaturePak connector pin no.
140	DIO A0	1	2	DIO A1	139
138	DIO A2	3	4	DIO A3	137
136	DIO A4	5	6	DIO A5	135
134	DIO A6	7	8	DIO A7	133
132	DIO B0	9	10	DIO B1	131
130	DIO B2	11	12	DIO B3	129
128	DIO B4	13	14	DIO B5	127
126	DIO B6	15	16	DIO B7	125
124	DIO C0	17	18	DIO C1	123
122	DIO C2	19	20	DIO C3	121
120	DIO C4	21	22	DIO C5	119
118	DIO C6	23	24	DIO C7	117
116	DIO D0	25	26	DIO D1	115
114	DIO D2	27	28	DIO D3	113
112	DIO D4	29	30	DIO D5	111
110	DIO D6	31	32	DIO D7	109
108	DIO E0	33	34	DIO E1	107
106	DIO E2	35	36	DIO E3	105
104	DIO E4	37	38	DIO E5	103
102	DIO E6	39	40	DIO E7	101
100	PWM0 / DIO F0	41	42	DIO F1 / PWM1	99
98	PWM2 / DIO F2	43	44	DIO F3 / PWM3	97
96	DIO F4	45	46	DIO F5	95
94	Latch- / DIO F6	47	48	DIO F7 / Ack-	93
92	+3.3V	49	50	Dground	91

Signal Name	Definition
DIO A7-A0	Digital I/O port A; byte direction programmable
DIO B7-B0	Digital I/O port B; byte direction programmable
DIO C7-C0	Digital I/O port C; byte direction programmable
DIO D7-D0	Digital I/O port D; byte direction programmable
DIO E7-E0	Digital I/O port E; bit direction programmable
DIO F7-F0	Digital I/O port F; bit direction programmable Port F signals have auxiliary functions enabled with control registers:
PWM0-3	32-bit programmable pulse width modulation outputs
Latch- / Ack-	DIO latch and acknowledge signals to enable DIO with handshaking; Latch- also serves as a digital input signal to drive a user-controlled interrupt.
Dground	Digital ground

6.2 FP-GPIO96 Pinout

6.2.1 Port A

FeaturePak connector pin no.	Port A pin number		FeaturePak connector pin no.
230	Ctr 0 In / DIO A0	1	2	DIO A1 / Ctr 0 Gate	229
226	Ctr 1 In / DIO A2	3	4	DIO A3 / Ctr 1 Gate	225
222	Ctr 2 In / DIO A4	5	6	DIO A5 / Ctr 2 Gate	221
218	Ctr 3 In / DIO A6	7	8	DIO A7 / Ctr 3 Gate	217
214	Ctr 4 In / DIO B0	9	10	DIO B1 / Ctr 4 Gate	213
210	Ctr 5 In / DIO B2	11	12	DIO B3 / Ctr 5 Gate	209
206	Ctr 6 In / DIO B4	13	14	DIO B5 / Ctr 6 Gate	205
202	Ctr 7 In / DIO B6	15	16	DIO B7 / Ctr 7 Gate	201
198	Ctr 0 Out / DIO C0	17	18	DIO C1 / Ctr 1 Out	197
194	Ctr 2 Out / DIO C2	19	20	DIO C3 / Ctr 3 Out	193
190	Ctr 4 Out / DIO C4	21	22	DIO C5 / Ctr 5 Out	189
186	Ctr 6 Out / DIO C6	23	24	DIO C7 / Ctr 7 Out	185
182	DIO D0	25	26	DIO D1	181
178	DIO D2	27	28	DIO D3	177
174	DIO D4	29	30	DIO D5	173
170	DIO D6	31	32	DIO D7	169
166	DIO E0	33	34	DIO E1	165
162	DIO E2	35	36	DIO E3	161
160	DIO E4	37	38	DIO E5	159
158	DIO E6	39	40	DIO E7	157
156	PWM 0 / DIO F0	41	42	DIO F1 / PWM 1	155
154	PWM 2 / DIO F2	43	44	DIO F3 / PWM 3	153
152	WDT In / DIO F4	45	46	DIO F5 / WDT Out	151
150	DIO F6	47	48	DIO F7 / Interrupt In	149
148	+3.3V	49	50	Ground	147

Signal Name	Definition
DIO A7-A0	Digital I/O port A
DIO B7-B0	Digital I/O port B
DIO C7-C0	Digital I/O port C; also functions as counter/timers 0-1 and PWM 0-1
DIO D7-D0	Digital I/O port D; also functions as counter/timers 2-3 and PWM 2-3
DIO E7-E0	Digital I/O port E; also functions as counter/timers 4-5 and interrupt input
DIO F7-F0	Digital I/O port F; also functions as counter/timers 6-7 and watchdog timer I/O
In 1-10	Counter input signals
Gate 1-10	Counter gate signals
Out 1-10	Counter output signals
PWM3-0	Pulse width modulator outputs
WDTOUT, WDTIN	Watchdog timer I/O signals
Interrupt	Interrupt input
+3.3V	3.3V power from system
Ground	Digital ground

6.2.2 Port B

FeaturePak connector pin no.		Port B pin number			FeaturePak connector pin no.
140	DIO G0	1	2	DIO G1	139
138	DIO G2	3	4	DIO G3	137
136	DIO G4	5	6	DIO G5	135
134	DIO G6	7	8	DIO G7	133
132	DIO H0	9	10	DIO H1	131
130	DIO H2	11	12	DIO H3	129
128	DIO H4	13	14	DIO H5	127
126	DIO H6	15	16	DIO H7	125
124	DIO J0	17	18	DIO J1	123
122	DIO J2	19	20	DIO J3	121
120	DIO J4	21	22	DIO J5	119
118	DIO J6	23	24	DIO J7	117
116	DIO K0	25	26	DIO K1	115
114	DIO K2	27	28	DIO K3	113
112	DIO K4	29	30	DIO K5	111
110	DIO K6	31	32	DIO K7	109
108	DIO L0	33	34	DIO L1	107
106	DIO L2	35	36	DIO L3	105
104	DIO L4	37	38	DIO L5	103
102	DIO L6	39	40	DIO L7	101
100	DIO M0	41	42	DIO M1	99
98	DIO M2	43	44	DIO M3	97
96	DIO M4	45	46	DIO M5	95
94	DIO M6	47	48	DIO M7	93
92	+3.3V	49	50	Ground	91

Signal Name	Definition
DIO G7-G0	Digital I/O port G; byte direction programmable, buffered
DIO H7-H0	Digital I/O port H; byte direction programmable, buffered
DIO J7-J0	Digital I/O port J; byte direction programmable, buffered
DIO K7-K0	Digital I/O port K; byte direction programmable, buffered
DIO L7-L0	Digital I/O port L; byte direction programmable, buffered
DIO M7-M0	Digital I/O port M; byte direction programmable, buffered
+3.3V	3.3V power from system
Ground	Digital ground