DIAMOND SYSTEMS CORPORATION

HERCULES-EBX™

High Integration EBX CPU
with Ethernet and Data Acquisition

Model HRC 400-SA 128

User Manual

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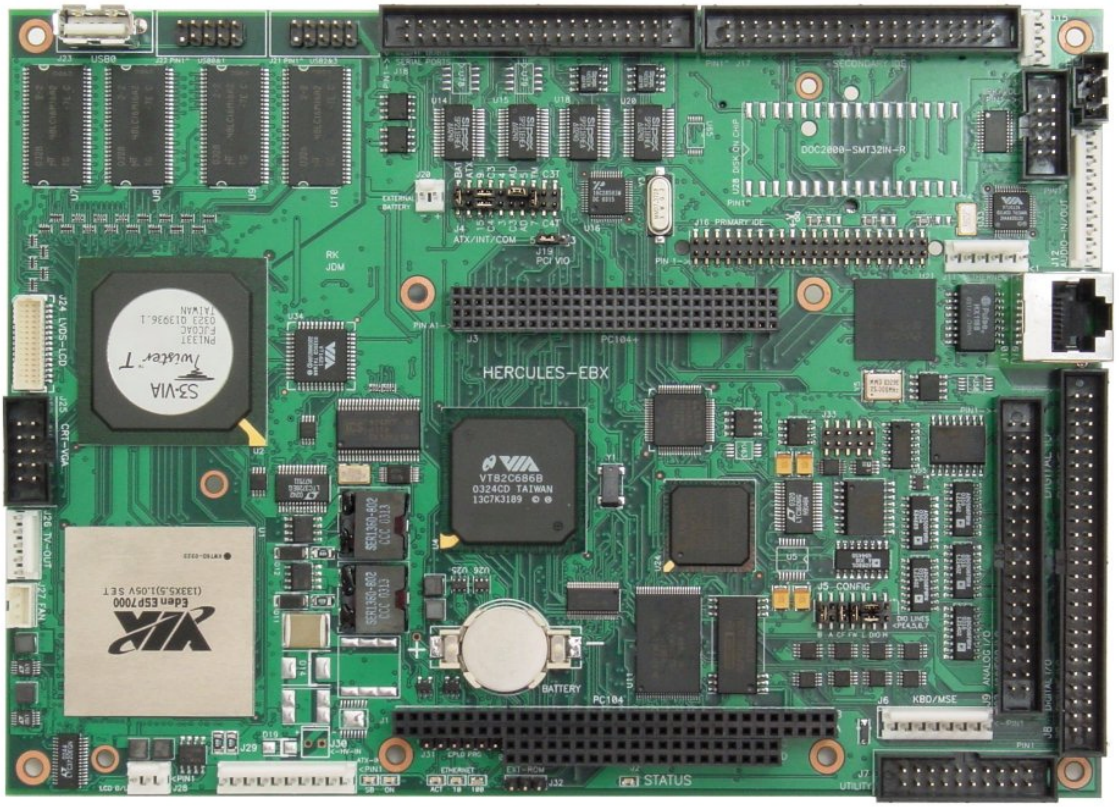
Revision 1.00



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1. DESCRIPTION

Hercules is an embedded CPU board in an EBX form factor that integrates a complete embedded PC, consisting of the following subsystems onto a single compact board:

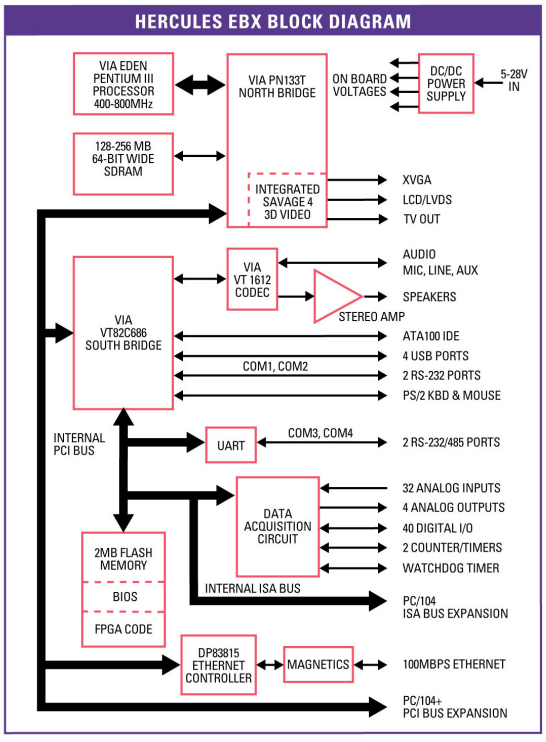
- CPU
- Core PC Chipset (including memory controller, PCI interface, and ISA interface)
- Video
- Sound
- Ethernet
- Analog I/O

A detailed list of features is shown on the next page.

Hercules-EBX conforms to the EBX standard with expansion support via PC/104+, an embedded standard that is based on the ISA and PCI buses and provides a compact, rugged mechanical design for embedded systems. PC/104 modules feature a pin and socket connection system in place of card edge connectors, as well as mounting holes for stand-offs in each corner. The result is an extremely rugged computer system fit for mobile and miniature applications. PC/104 modules stack together with 0.6" spacing between boards (0.662" pitch including the thickness of the PCB). A mechanical drawing of a standard PC/104 board is shown on page 122.

For more information on PC/104, visit www.pc104.org.

Hercules-EBX uses the PCI bus internally to connect the Ethernet circuit to the processor. It uses the ISA bus internally to connect serial ports 3 and 4, as well as the data acquisition circuit, to the processor. Both the ISA and PCI buses are brought out to expansion connectors for the connection of add-on boards. Diamond Systems manufactures a wide variety of compatible PC/104 add-on boards for analog I/O, digital I/O, counter/timer functions, serial ports, and power supplies.



2. FEATURES

System Features

Processor Section

- Via Eden Processor running at 400MHz with integrated math co-processor
- Pentium-class platform including SDRAM and PCI-based IDE controller and USB

Core System

- 128MB SDRAM system memory (standard)
- 100MHz memory bus
- 2MB 16-bit wide integrated flash memory for BIOS and user programs
- 2D VGA Video graphics engine (VESA-style VGA output with DDC Monitor support)
- 33MHz PCI Bus

I/O

- 4 serial ports, 115.2kbaud max
  - 2 ports 16550-compatible
  - 2 ports 16850-compatible with 128-byte FIFOs and RS485 capability
- 4 full-featured powered USB ports
- 2 IDE drive connectors (standard 40-pin IDE and 44-pin version for notebook drives)
- Accepts solid-state flash disk modules directly on board
- 10/100 BaseT full-duplex PCI bus mastering Ethernet (100Mbps or 10Mbps)
- IrDA port (requires external transceiver)
- PS/2 keyboard and mouse ports
- LEDs
- Interface for speaker and additional external LEDs

System Features

- Plug and play BIOS with IDE auto detection, 32-bit IDE access, and LBA support
- Built-in fail-safe boot ROM for system recovery in case of BIOS corruption
- User-selectable COM2 terminal mode
- On-board lithium backup battery for real-time-clock and CMOS RAM
- ATX power switching capability
- Programmable watchdog timer
- Wide input (5V – 28V) power supply*
- Extended temperature range operation (-40 to +85^{o}C)

* - limitations apply below 6V input

Data Acquisition Subsystem

Analog Input

- 32 single-ended / 16 differential inputs, 16-bit resolution
- 250KHz maximum aggregate A/D sampling rate
- Programmable input ranges/gains with maximum range of ±10V / 0-10V
- Both bipolar and unipolar input ranges
- 5 ppm/^{o}C drift accuracy
- Internal and external A/D triggering
- 2048-sample FIFO for reliable high-speed sampling and scan operation

Analog Output

- 4 analog outputs, 12-bit resolution
- ±10V and 0-10V output ranges
- Simultaneous update
- Adjustable output range (optional)

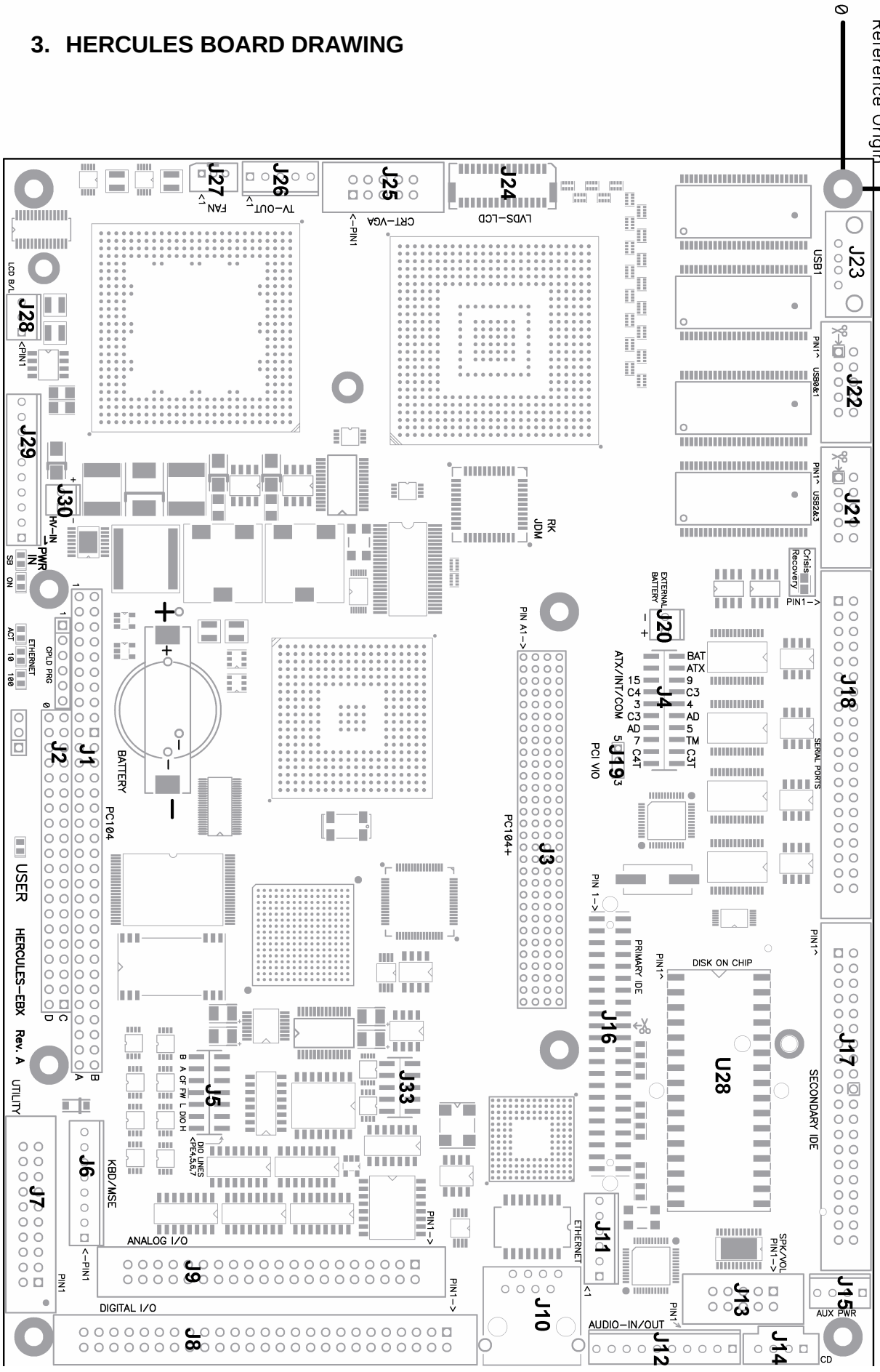
Digital I/O

- 32 programmable digital I/O, 3.3V and 5V logic compatible
- Enhanced output current capability: –8/+12mA max
- Selectable pull-up/down resistors on board

Counter/Timers

- 1 24-bit counter/timer for A/D sampling rate control
- 1 16-bit counter/timer for user counting and timing functions
- Programmable gate and count enable
- Internal and external clocking capability

3. HERCULES BOARD DRAWING



I/O Connectors with locations (pin 1 relative to upper-left mounting hole)

J1	PC/104 8-bit bus connector	(2.700, -5.050 in)
J2	PC/104 16-bit bus connector	(3.500, -5.250 in)
J3	PC/1-4+ PCI bus connector	(3.100, -2.112 in)
J6	PS/2 Header	(6.945, -5.015 in)
J7	Utility Header	(7.240, -5.320 in)
J8	Data Acquisition Digital I/O Header	(7.570, -2.620 in)
J9	Data Acquisition (Analog) Header	(7.121, -2.829 in)
J10	Ethernet (RJ45)	(7.284, -2.233 in)
J11	Ethernet (Header)	(7.200, -1.610 in)
J12	Audio I/O Header	(7.680, -0.730 in)
J13	Speaker Header	(7.300, -0.460 in)
J14	CD Input Header	(7.680, -0.260 in)
J15	External Power Connector (out)	(7.310, 0.130 in)
J16	Primary IDE (44-pin, laptop)	(4.833, -1.627 in)
J17	Secondary IDE (40-pin standard)	(5.060, -0.030 in)
J18	Serial Port I/O Connector	(2.730, -0.030 in)
J20	External Battery	(2.935, -1.177 in)
J21	USB2/3 Header	(1.910, -0.030 in)
J22	USB0/1 Header	(1.080, -0.030 in)
J23	USB1 Connector	(0.637, -0.031 in)
J24	LCD Panel connector	(0.132, -1.974 in)
J25	VGA Header	(0.040, -3.240 in)
J26	Video/TV Out Header	(-0.080, -3.920 in)
J27	CPU Fan	(-0.100, -4.240 in)
J28	LCD Backlight Header	(0.950, -5.430 in)
J29	Low-Voltage (5-28V) Input Power Header	(2.310, -5.430 in)
J30	High-Voltage Input Header <OPTIONAL>	(2.110, -5.170 in)
J34	CompactFlash (Bottom) <OPTIONAL>	(5.287, -1.343 in)

Configuration Jumper Blocks

J4	System configuration jumper block	(3.095, -1.267 in)
J5	Data acquisition configuration jumper block	(6.220, -4.105 in)
J33	Data Acquisition Test Points	(5.792, -3.015 in)

4. I/O HEADERS

All cables mentioned in this chapter are included in Diamond Systems' cable kit **C-HRCEBX-KIT**. These cables are further described in chapter 19. Some cables are also available individually.

4.1 PC/104 Bus Connectors

The PC/104 bus is essentially identical to the ISA Bus except for the physical design. It specifies two pin and socket connectors for the bus signals. A 64-pin header J1 incorporates the 62-pin 8-bit bus connector signals, and a 40-pin header J2 incorporates the 36-pin 16-bit bus connector signals. The additional pins on the PC/104 connectors are used as ground or key pins. The female sockets on the top of the board enable stacking A PC/104 board on top of the board. The Hercules-EBX board should be the bottom board of a PC/104 stackup.

In the pinout figures below, the tops correspond to the left edge of the connector when the board is viewed from the primary side (side with the CPU chip and the female end of the PC/104 connector) and the board is oriented so that the PC/104 connectors are along the bottom edge of the board.

View from Top of Board

J2: PC/104 16-bit bus connector

Ground	D0	C0	Ground
MEMCS16-	D1	C1	SBHE-
IOCS16-	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0-	D8	C8	LA17
DRQ0	D9	C9	MEMR-
DACK5-	D10	C10	MEMW-
DRQ5	D11	C11	SD8
DACK6-	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7-	D14	C14	SD11
DRQ7	D15	C15	SD12
+5V	D16	C16	SD13
MASTER-	D17	C17	SD14
Ground	D18	C18	SD15
Ground	D19	C19	Key (pin cut)

J1: PC/104 8-bit bus connector

IOCHCHK-	A1	B1	Ground
SD7	A2	B2	RESET
SD6	A3	B3	+5V
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	0WS-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	Key (pin cut)
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	Refresh-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	Ground
Ground	A32	B32	Ground

Table 1: J1,J2 – PC/104 Connector Pinouts

4.2 PC/104+ Bus Connector

J3/P3				
Pin	**A**	**B**	**C**	**D**
1	GND/5.0V KEY[2]	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY[2]

Table 2: J3 – PC/104+ Connector Pinout

The PC/104+ bus is essentially identical to the PCI Bus except for the physical design. It specifies a single pin and socket connector for the bus signals. A 120-pin header J3, arranged as 4 30-pin

rows, incorporates a full 32-bit, 33MHz PCI Bus. The additional pins on the PC/104+ connectors are used as ground or key pins. The female sockets on the top of the board enable stacking another PC/104+ board on top of the board. The Hercules-EBX board should be the bottom board of a PC/104+ stackup.

In the pinout figures above, the top corresponds to the left edge of the connector when the board is viewed from the primary side (side with the CPU chip and the female end of the PC/104+ connector) and the board is oriented so that the PC/104 connectors are along the bottom edge of the board and the PC/104+ connector is in the center of the Hercules-EBX board.

NOTE:

The PCI board interface is designed to allow different voltage-levels for the signaling interface. The problem to be avoided in defining a keying mechanism within the specification was to prevent a 3.3V-only device which is not 5V tolerant from receiving signals that are at a 5V signal rail. In a standard PCI interface, this is handled by blocking a portion of the edge connector such that the female connector is keyed as either “3.3V” or “5V”. The intention in doing this was to provide a way to prevent a 3.3V-only card in a 5V system. Many vendors chose to implement a “universal” edge connector that could fit into either configuration – this was typically done in one of two ways:

1) Use 3.3V signaling that is 5V-tolerant; or

2) Use the VIO pins on the PCI edge connector to power the I/O drive circuitry (or the maximum voltage overshoot protection circuitry) on the card.

From a system perspective, the primary question is: which standard can you support? Many card vendors chose to implement a specific standard (such as “5V only”) and then connect the VIO signals to the internal power rail (such as “5V”) signals on the PCI edge connector. While this is a violation of the more recent PCI specification, it was also relatively common, especially for card developers who began developing PCI cards before the standard was updated for 3.3V support.

On the Hercules-EBX, all of the PCI circuitry is driven with 3.3V circuitry, but all of the circuitry is 5V tolerant. Given this, the Hercules-EBX main board can support either 3.3V or 5V-only cards. For this reason, the connector is not keyed (to prevent one or the other types of cards from being inserted). Rather, the main EBX board allows you to select which I/O voltage to use for a given PC/104+ card (or set of cards).

Many PC/104+ cards are universal, in which case the voltage setting will not matter (provided that it is set to either 3.3V or 5V). For cards that have a definite requirement, make sure that the VIO jumper is set to the appropriate position. See page 36 for the details on this setting.

As per the specification, a 5V-only card can be recognized by the keying postion at location A1 (they have male pin A1 cut and female location A1 should be blocked).

Similarly, cards that are to have 3.3V power should have pin D30 cut (and female location D30 plugged).

Cards without either keying mechanism should be “universal” and should work with either I/O voltage provided.

DO NOT MIX cards that have different I/O keying requirements (i.e., do not stack a card that has pin A1 cut with a card that has pin D30 cut).

4.3 PS/2 Connector – J6

An 8-pin connector is provided for PS/2 Mouse and keyboard. This connector mates with Diamond Systems' cable no. 698022, which terminates the cable to two PS/2 Female connectors. The connections are:

1	+5V In	Keyboard PS/2 : pin 4
2	Keyboard Data	Keyboard PS/2 : pin 1
3	Keyboard Clock	Keyboard PS/2 : pin 5
4	Ground	Keyboard PS/2 : pin 3
5	+5V In	Mouse PS/2 : pin 4
6	Mouse Data	Mouse PS/2 : pin 1
7	Mouse Clock	Mouse PS/2 : pin 5
8	Ground	Mouse PS/2 : pin 3

Table 3: J6 - PS/2 Connector Pinout

Note: 2 and 6 on the Mini-Din-6 PS/2 connectors are unused.

Connector Part Numbers

J6 plug on CPU board:	Digikey 640456-8
Mating Connector for J6 (Cable-mount socket):	Molex 22-01-3087
PS/2 Connector:	CUI MD60SP

4.4 Utility Connector – J7

A 20-pin connector provides access to the standard button/LED connections:

Ground	1	2	Reset Key
Ground	3	4	Power Button
Network : Activity LED	5	6	+3.3V Standby
Network : 100MBit link	7	8	+3.3V Standby
+5V In	9	10	IDE LED
Power LED	11	12	External Battery
Watch Dog Timer - Input	13	14	Ground
SPEAKER	15	16	Watch Dog Timer - Output
+5V In	17	18	IRTX (IR Transmit)
IRRX (IR Receive)	19	20	Ground

Table 4: J7 - Utility Connector Pinout

Notes on J7 Signals

Reset Key — Connection between this pin and Ground will generate a Reset condition. The board will be in a reset state (with non-standby power rails disabled) until "Reset Key" is removed from ground.

ATX Power Button — This should be tied to ground whenever the "Power Button" is to be depressed. The "Power Button" has different functionality, depending on the current system mode (as well as what software is currently in operation). In general,

- If the board is powered down, then toggling (i.e., tie to ground briefly, then release) this button turns the system on, causing all non-standby voltages to become active. NOTE: depending on the default configuration, the system will usually power-up immediately as power is applied.

- If the system is currently powered up and active, then toggling (i.e., tie to ground briefly, then release) this button will cause a system power-down event to be initiated. Typically, this will power-down the monitor, hard drive, and any other non-essential functions. The system must be operating for this to function; this will not function at all if software is not executing (crash).

  Under Windows (and some other OSes), this power-down event may cause the system to shut down. Typically, this is software-configurable via an option setting for the given OS.

- If the system is currently powered up and active, then holding this button for 4 seconds will cause a forced system shutdown. This is a hardware power-down, which can be detrimental to many OSes due to the fact that they are not given adequate time to initiate shut-down sequencing. This should only be used in dire circumstances when the system itself is locked up (due to system instability or a software crash, for example). After powering the system down in this manner, the system will remain powered down until the power button is toggled (tied to ground again and released).

When ATX is enabled, a momentary contact between this pin and Ground causes the CPU to turn on and a contact of 4 seconds or longer will generate a power shutdown. ATX power control is enabled with a jumper on jumper block J4 (see page 33).

+5V — This pin is a switched power pin that is turned on and off with the ATX power switch or with the +5V input.

+3.3V Standby — This pin is a special “standby voltage” that is provided, regardless of system power-down mode. This voltage will be present anytime the system has power connected, regardless of current system power-down state. This voltage is not intended as a major power-source for external devices; it is intended to allow external display of current system power status. This power supply should not be used unless absolutely necessary; in that case, it should only be used as a source for LED display (or similar power draw).

Network: Activity LED — This pin provides a signal that is the same as the LED marked “ACT” on the main board. It lights during receive or transmit activity on the Ethernet connection. An LED should be tied between power and this pin

Network: 100MBit link — This pin provides a signal that is the same as the LED marked “100” on the main board. It lights whenever a 100MBit Ethernet link is established. An LED should be tied between power and this pin.

IDE LED — Referenced to +5V Out. Requires a series resistor. Connect LED directly between this pin and resistor (to +5V).

Power LED — Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out. Note that this displays the system main power; if the system is in a power-down mode, this LED may be inactive while the system is still receiving power to its standby voltage sources.

Speaker — The signal on this pin is referenced to +5V Out. Connect a speaker between this pin and +5V Out.

IR Receive / Transmit — These pins are used for IrDA functions. They should be connected to an external IrDA transceiver, when needed. IR communications require that COM PORT 2 be set for "IR" mode for the IR serial port functionality to be active.

External Battery — This pin is an additional power connection for an external +3V power source (in addition to connector J20). Note that these two sources are not directly connected and may both be driven by separate external battery power sources. Typical power draw from this battery source will average under 4uA of current.

Watchdog Input/Output — These signals are signals are used in conjunction with the on-board FPGA and Data Acquisition circuitry to provide full watchdog timer functionality. See page 42 for details on these capabilities.

Connector Part Numbers

J7 plug on CPU board:	PHYCO 2120-20S	
Both cable-mount and board-mount connectors are available to mate with J7:		
Cable-mount socket:	Phyco 1100-10	
Board-mount socket:	Samtec	SSM-112-S-DV-A or
	Oupiin	2043-2X12TDP

4.5 Data Acquisition (Digital I/O) Connector – J8 (For Models with Data Acquisition)

Hercules-EBX Models with Data Acquisition include a 50-pin header labeled J8 for all digital data acquisition I/O. This header is located on the right side of the board. Pin 1 is the lower right pin and is marked on the board. Diamond Systems' cable no. **C-50-18** provides a standard 50-pin connector at each end and mates with this header.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
DIO C0	17	18	DIO C1
DIO C2	19	20	DIO C3
DIO C4	21	22	DIO C5
DIO C6	23	24	DIO C7
DIO D0	25	26	DIO D1
DIO D2	27	28	DIO D3
DIO D4	29	30	DIO D5
DIO D6	31	32	DIO D7
DIO E0 / PWM0	33	34	DIO E1 / PWM1
DIO E2 / PWM2	35	36	DIO E3 / PWM3
DIO E4 / GATE1	37	38	DIO E5 / TOUT1
DIO E6 / DIOLATCH	39	40	DIO E7 / GATE0
EXTTRIG	41	42	TOUT0
ACK	43	44	WDI
WDO	45	46	FXA
FXB	47	48	FXB
+5V	49	50	Digital Ground

Table 5: J8 – Data Acquisition (DIO) Header Pinout

Signal Name	Definition
DIO A7-A0	Digital I/O port A; programmable direction
DIO B7-B0	Digital I/O port B; programmable direction
DIO C7-C0	Digital I/O port C; programmable direction
DIO D7-D0	Digital I/O port D; programmable direction
DIO E7-E0	Digital I/O port E; programmable direction
Note : E3-E0 may be configured for PWM signals; see page 102	
PWM3-PWM0	Pulse-Width Modulation Outputs (4 independent channels)
Note : E7-E4 may be configured for counter/timer signals; see page 96	
GATE 1-0	Gate inputs for Counter/Timer 1 and 0
TOUT1	Counter/Timer 1 output
DIOLATCH	Handshaking line used (with ACK signal below) for automated digital data transfers
Ext Trig	External A/D trigger input
Tout 0	Counter/Timer 1 output
+5V Out	Connected to switched +5V supply (output only! Do not connect to external supply)
Digital Ground	Digital ground (0V - reference); used for digital circuitry only

WDO	Watchdog Timer Output (from Hercules-EBX board)
WDI	Watchdog Timer Input (to Hercules-EBX board)
ACK	Handshaking line used (with DIOLATCH signal) for automated digital data transfers
FXA, FXB	These lines should be left unconnected

NOTE: The watchdog timer circuit is described on page 42 of this manual. It may be programmed directly or with Diamond Systems' Universal Driver software.

Connector Part Numbers

J8 plug on CPU board: Phyco 2120-50S

Ribbon Cable Plug: Standard 2x25 0.1" female ribbon cable header

4.6 Data Acquisition (Analog I/O) Connector – J9 (Models with Data Acquisition Only)

Single-Ended			
Vout 0	1	2	Vout 1
Vout 2	3	4	Vout 3
Output Ground	5	6	Output Ground
Vin 0	7	8	Vin 16
Vin 1	9	10	Vin 17
Vin 2	11	12	Vin 18
Vin 3	13	14	Vin 19
Vin 4	15	16	Vin 20
Vin 5	17	18	Vin 21
Vin 6	19	20	Vin 22
Vin 7	21	22	Vin 23
Vin 8	23	24	Vin 24
Vin 9	25	26	Vin 25
Vin 10	27	28	Vin 26
Vin 11	29	30	Vin 27
Vin 12	31	32	Vin 28
Vin 13	33	34	Vin 29
Vin 14	35	36	Vin 30
Vin 15	37	38	Vin 31
Input Ground	39	40	Input Ground

Differential			
Vout 0	1	2	Vout 1
Vout 2	3	4	Vout 3
Output Ground	5	6	Output Ground
Vin 0 +	7	8	Vin 0 -
Vin 1 +	9	10	Vin 1 -
Vin 2 +	11	12	Vin 2 -
Vin 3 +	13	14	Vin 3 -
Vin 4 +	15	16	Vin 4 -
Vin 5 +	17	18	Vin 5 -
Vin 6 +	19	20	Vin 6 -
Vin 7 +	21	22	Vin 7 -
Vin 8 +	23	24	Vin 8 -
Vin 9 +	25	26	Vin 9 -
Vin 10 +	27	28	Vin 10 -
Vin 11 +	29	30	Vin 11 -
Vin 12 +	31	32	Vin 12 -
Vin 13 +	33	34	Vin 13 -
Vin 14 +	35	36	Vin 14 -
Vin 15 +	37	38	Vin 15 -
Input Ground	39	40	Input Ground

Table 6: J9 – Data Acquisition (Analog I/O) Header Pinout

Signal Name	Definition
Vout3-0	Analog output channels 3 – 0
Output Ground	Analog ground; 0V reference for VOut3 - 0
Vin 31 ~ Vin 0	Analog input channels 31 – 0 in single-ended mode
Vin 15 + ~ Vin 0 +	High side of input channels 15 – 0 in differential mode
Vin 15 - ~ Vin 0 -	Low side of input channels 15 – 0 in differential mode
Input Ground	Analog ground; 0V reference for VIn31 - 0

NOTE: These reference grounds are NOT decoupled from the power grounds – they are indirectly connected to the power supply input (and other on-board ground/0V references). Do not assume that these grounds are floating; do not apply a high-voltage input (relative to the power input ground) to these ground signals or to any other board I/O pin.

Connector Part Numbers

J9 plug on CPU board:	Phyco	2120-40S
Ribbon Cable Plug:	Standard 2x20 0.1" female ribbon cable header	

4.7 Ethernet – J10 / J11

1	Common
2	RX-
3	Common
4	RX+
5	TX-
6	TX+

Table 7: J11 – Ethernet Header Pinout

J11 is a 1x6 pin header. It mates with Diamond Systems' cable no. **698002**, which provides a panel-mount RJ-45 jack for connection to standard CAT5 network cables.

J10, which may be used instead of J11, provides an on-board RJ45. For development, J10 may be more useful, but it is anticipated that most embedded applications will make the J11 connection more useful (for panel-mount network connection).

Ensure that only one connection or the other (J11 or J10) is used; both connectors are NOT independent and neither will function if they are both attached.

Connector Part Numbers

J10 RJ45 Receptacle on CPU board:	Capsco Sales, Inc.	GD-PNS-88
J11 plug on CPU board:	Digi-Key Corp.	640456-6

Mating connectors:

J10 RJ45 Connector:	Standard RJ45 (Ethernet patch cable)
J11 Cable Connector:	MOLEX # 16-02-0096

4.8 Audio I/O Connector – J12

1	LEFT Headphone / Line Out
2	RIGHT Headphone / Line Out
3	Audio Ground
4	LEFT Line Input
5	RIGHT Line Input
6	LEFT AUX Input
7	RIGHT AUX Input
8	Audio Ground
9	Power Reference for Microphone
10	Microphone Input

Table 8: J12 – Audio I/O Connector Pinout

Signal Name	Definition
Headphone / Line Out	Line Level output, capable of driving headphones

	Referred to as “Headphone Out” in most sound documentation
Line Input	Line-Level input; referred to as “Line In” in most sound documentation
Auxiliary Input	Line-Level input; referred to as “AUX In” in most sound documentation
Microphone Input	Microphone-level mono input; phantom power provided via pin 9

The sound chip used is AC97-compatible. The “Line Out” is powered and used for the amplified speaker output (See J13 below). The line-level output listed above is listed as either “Headphone Out” or “Line Out 2” in most of the software and documentation for this sound interface.

Connector Part Numbers

J12 Connector on CPU board:	Digi-Key Corp.	A1925
J12 Mating Cable Connector:	Molex	22-01-3107

4.9 Speaker Connector – J13

1	Speaker LEFT High (+)
2	Volume – LOW
3	Speaker LEFT Low (-)
4	Volume – MID
5	Line-level Mono Output
6	Audio Ground
7	Speaker RIGHT Low (-)
8	Volume – HIGH
9	Speaker RIGHT High (+)
10	No-Connect

Table 9: J13 – Amplified Speaker Connector Pinout

Signal Name	Definition
Speaker LEFT +/-	Speaker Connection Pair for LEFT speaker (4 Ohm Speaker)
Speaker RIGHT +/-	Speaker Connection Pair for RIGHT speaker (4 Ohm Speaker)
Mono Output	Line-Level mono output (for reference)
Volume – LOW, MID, HIGH	These are volume controls for the attached speakers.

NOTES:

- Volume Control: The volume control is capable of 32 discrete levels, ranging from a 20dB maximum gain down to -85dB (Muted). The main volume control is the “MID” line: this may be tied to the center tap of a potentiometer with “HIGH” on one side and “LOW” on the other to give a full range of power control.
    - Shorting “MID” to “LOW” will mute the speaker audio.
    - Shorting “MID” to “HIGH” will provide maximum gain.
    - Default (with no connection) provides 10dB of gain.
- Maximum Output Power: The maximum output power is specified to provide up to 2 Watts into a 4 Ohm speaker load. Note that this output power is drawn from the on-board 5V supply.
- Speakers: The speakers are driven using a Bridged-Tied Load (BTL) amplifier configuration. This is a differential speaker connection. As such, each speaker should be wired directly to the appropriate pair of connections for that speaker:
    - Do not connect the speaker low sides (-) to ground; and

- Do not short the speaker low connections together.

Connector Part Numbers

J13 Connector on CPU board:	Standard 2x5, 0.1" Box header
J13 Mating Cable Connector:	Phyco 1100-10

4.10 CD Input Connector – J14

J14 provides a connector for a PC-standard CD input cable.

1	LEFT CD Input
2	Left Ground
3	Right Ground
4	RIGHT CD Input

Table 10: J14 – CD Input Connector Pinout

J14 provides the CD Audio Input to the AC97 Sound circuitry. The connector is an industry-standard CD-IN connector, as is common in most desktop Personal Computers. Note that the left and right grounds are decoupled, but are also tied together on-board. This input is intended for CD-input only (i.e., no amplified or microphone inputs).

Connector Part Numbers

J14 Connector on CPU board:	Molex 70543-0003
J14 Mating Cable Connector:	Standard (PC) CD Audio cable

4.11 External Auxiliary Power Connector – J15

1	+5V (Switched)
2	Ground
3	Ground
4	+12V (Switched)

Table 11: J15– Auxiliary Power Connector Pinout

Signal Name	Definition
+5V	This is provided by the on-board power supply, derived from the input power. It is switched off when the board is powered down.
+12V	This is provided by the 12V input pin on the main power connector (See J29). It is switched off when the board is powered down.
Ground	These are 0V ground references for the power output voltage rails above.

J15 provides switched power for use with external drives. If ATX is enabled, the power is switched on and off with the ATX input switch. If ATX is not enabled, the power is switched on and off in conjunction with the external power.

Diamond Systems' cable no. **698006** mates with J15. It provides a standard full-size power connector for a hard drive or CD-ROM drive and a standard miniature power connector for a floppy drive.

Connector Part Numbers

J15 Connector on CPU board: Digi-Key Corp. 640456-4

J15 Mating Cable Connector: Molex 22-01-3047

4.12 Primary IDE (44-pin) – J16

RESET-	1	2	Ground
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
Ground	19	20	Key (Not Used)
DRQ	21	22	Ground
IDEIOW-	23	24	Ground
IDEIOR-	25	26	Ground
IORDY	27	28	Ground
DACK-	29	30	Ground
IRQ14	31	32	Pulled low for 16-bit operation
A1	33	34	Not Used
A0	35	36	A2
CS0-	37	38	CS1-
LED-	39	40	Ground
+5V	41	42	+5V
Ground	43	44	Not Used

Table 12 : J16 – Primary IDE Connector Pinout

J16 is a 2x22 (44-pin) 2mm-pitch pin header. It mates with Diamond Systems' cable no. **698004**, and may be used to connect up to 2 IDE drives (hard disks, CD-ROMs, or flash disk modules). The 44-pin connector includes power and mates directly with notebook drives and flash disk modules. To use a standard format hard disk or CD-ROM drive with a 40-pin connector, an adapter PCB such as Diamond Systems' ACC-IDEEXT is required.

Note that J16 supports only up to ATA-33 (UDMA-2); it does not support ATA-66 (UDMA-3 to 5) transfer modes.

Connector Part Numbers

J16 Connector on CPU board: All American Semiconductor 2115-2X22GDP/PPTB

J16 Mating Cable Connector: AMP 1-111626-0

(Note: Pin 20 should be keyed - removed from J16 on board and plugged for ribbon cable)

4.13 Secondary IDE (40-pin) – J17

RESET-	1	2	Ground
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
Ground	19	20	Key (Not Used)
DRQ	21	22	Ground
IDEIOW-	23	24	Ground
IDEIOR-	25	26	Ground
IORDY	27	28	Ground
DACK-	29	30	Ground
IRQ14	31	32	Pulled low for 16-bit operation
A1	33	34	Not Used
A0	35	36	A2
CS0-	37	38	CS1-
LED-	39	40	Ground

Table 13: J17 – Secondary IDE Connector Pinout

J17 is an IDE standard 2x20 (40-pin) 0.1-pitch pin header. It mates with Diamond Systems' UDMA cable no. **698026**, and may be used to connect up to 2 IDE drives (hard disks, CD-ROMs or other IDE/ATAPI devices). The 40-pin connector must mate with this 80-conductor UDMA cable for maximum performance. J17 fully supports up to ATA-100 (UDMA Mode 5), provided that an appropriate UDMA (80-conductor) cable is used.

Note that the cable type will automatically be detected by the BIOS and the transfer speed will be limited appropriately, as necessary.

Connector Part Numbers

J17 Connector on CPU board: Phyco 2120-40S (with pin 20 removed)

J17 Mating Cable Connector: Standard (PC) UDMA/100 cable

(Note: Pin 20 should be keyed - removed from J16 on board and plugged for ribbon cable)

4.14 Serial Port I/O Connector – J18

J18 is 40-pin header that provides access to the 4 on-board serial ports for Hercules-EBX. The first two serial ports are always configured to meet RS232 standards; the last two serial ports are software configurable as either RS232 or RS485. All four serial ports are independently enabled and the last two serial ports can be independently configured between the two modes of operation (RS232 versus RS485).

Diamond Cable Assembly Number **C-DB9M-4** connects this header to 4 DE-9 Male connectors (for direct connection to RS232C signaling). The following tables list the signals for the appropriate mode of operation, as well as the DE-9 pin numbers to which these signals are wired.

Port 1	DCD 1	**1**	**2**	DSR 1
	RXD 1	**3**	**4**	RTS 1
	TXD 1	**5**	**6**	CTS 1
	DTR 1	**7**	**8**	RI 1
	GND	**9**	**10**	N/C
Port 2	DCD 2	**11**	**12**	DSR 2
	RXD 2	**13**	**14**	RTS 2
	TXD 2	**15**	**16**	CTS 2
	DTR 2	**17**	**18**	RI 2
	GND	**19**	**20**	N/C
Port 3	DCD 3	**21**	**22**	DSR 3
	RXD 3	**23**	**24**	RTS 3
	TXD 3	**25**	**26**	CTS 3
	DTR 3	**27**	**28**	RI 3
	GND	**29**	**30**	N/C
Port 4	DCD 4	**31**	**32**	DSR 4
	RXD 4	**33**	**34**	RTS 4
	TXD 4	**35**	**36**	CTS 4
	DTR 4	**37**	**38**	RI 4
	GND	**39**	**40**	N/C

Table 14: J18 – RS232 Serial Port Connector Pinout

Signal Name	Definition	DE-9 Pin	Direction
RS-232C:			
DCD	Data Carrier Detect	pin 1	Input
DSR	Data Set Ready	pin 6	Input
RXD	Receive Data	pin 2	Input
RTS	Request To Send	pin 7	Output
TXD	Transmit Data	pin 3	Output
CTS	Clear To Send	pin 8	Input
DTR	Data Terminal Ready	pin 4	Output
RI	Ring Indicator	pin 9	Input
N/C	Not Connected	---	---

RS-485 Configuration:

Port 1		1	2	
		3	4	
		5	6	
		7	8	
		9	10	
Port 2		11	12	
		13	14	
		15	16	
		17	18	
		19	20	
Port 3	NC	**21**	**22**	NC
	TXD/RXD+ 3	**23**	**24**	TXD/RXD- 3
	GND	**25**	**26**	NC
	NC	**27**	**28**	NC
	GND	**29**	**30**	DIO C
Port 4	NC	**31**	**32**	NC
	TXD/RXD+ 4	**33**	**34**	TXD/RXD- 4
	GND	**35**	**36**	NC
	NC	**37**	**38**	NC
	GND	**39**	**40**	DIO D

Table 15: J18 – RS485 Serial Port Connector Pinout

Signal Name	Definition	DE-9 Pin	Direction
RS-485:			
TXD/RXD+,	Differential Transceiver Data (HIGH)	pin 2	Bi-directional
TXD/RXD-	Differential Transceiver Data (LOW)	pin 7	Bi-directional

Connector Part Numbers

J18 Connector on CPU board: Phyco 2120-40S

J18 Mating Cable Connector: Standard 2x20 0.1" Female Ribbon cable header

4.15 External Battery Connector – J20

1	Batter input
2	Ground

Table 16: J20 – External Battery Input

The external battery voltage maintains the on-board Real-Time Clock, as well as the on-board CMOS settings (BIOS settings for various system configurations). The battery voltage for this input should be 3-3.5V. The current draw averages under 4uA at 3V. Note that the on-board battery, this battery, and an additional external battery input on the Utility Connector (J7 above) are all possible sources for this power. Whichever battery has the highest voltage will see the majority of the current draw, which is minimal regardless. Note that there must be a battery voltage input for the default power-up mode (see page 34).

Connector Part Numbers

J20 Connector on CPU board: Digi-Key Corp. A1921

J20 Mating Cable Connector: 2-pin female header

4.16 USB 2/3 and 0/1 Headers – J21, J22

Key (pin cut)	1	2	Shield
USBB Pwr-	3	4	USBA Pwr-
USBB Data+	5	6	USBA Data+
USBB Data-	7	8	USBA Data-
USBB Pwr+	9	10	USBA Pwr+

Table 17: J21 and J22 – USB Header Pinout

J21 and J22 are 2x5 pin headers. They mates with Diamond Systems' cable no. **698012**, which provides 2 standard USB type A jacks in a panel-mount housing. These headers support USB 1.1 support (10Mbps maximum transfer rates).

Note that USB1 is shared between J22 and J23 (an on-board USB connector). Use one or the other – do not connect USB devices to both USB1 on J22 and J23.

Connector Part Numbers

J21, J22 Connector on CPU board: Standard 2x5, 0.1" header (with pin 1 removed)
J21, J22 Mating Cable Connector: Oupiin 4072-2X5H (Standard PC USB Header Interface)

4.17 USB1 Connector- J23

1	USB1 Pwr+
2	USBA Data-
3	USBA Data+
4	USB1 Pwr-

Table 18: J23 – On-board USB Connector Pinout

J23 provides a single, quick and simple on-board USB connection for simple test and development without requiring an additional cable.

Note that USB1 is shared between J22 and J23 (an on-board USB connector). Use one or the other – do not connect USB devices to both USB1 on J22 and J23.

Connector Part Numbers

J23 Connector on CPU board: Capsco Sales, Inc. KUSB-AS-1-N-WHT
J23 Mating Cable Connector: Standard USB 1.1 type B connector

4.18 LCD Panel (LVDS Interface) Connector – J24

Ground	1	2	Ground
Y CLOCK -	3	4	Z CLOCK -
Y CLOCK +	5	6	Z CLOCK +
Ground	7	8	Ground
Y Data 0 -	9	10	Z Data 0 -
Y Data 0 +	11	12	Z Data 0 +
Ground	13	14	Ground
Y Data 2 -	15	16	Z Data 1 -
Y Data 2 +	17	18	Z Data 1 +
Ground	19	20	Ground
Y Data 1 -	21	22	Z Data 2 -
Y Data 1 +	23	24	Z Data 2 +
Ground	25	26	Ground
VDD (LCD Display)	27	28	VDD (LCD Display)
VDD (LCD Display)	29	30	VDD (LCD Display)

Table 19: J24 – LCD Connector Pinout

J24 provides access to the internal LVDS LCD display drivers. Note that the LCD also requires the backlight to be connected (J28 below) in order to function correctly.

Signal Name	Definition
Y Data 2-0 +/-	Primary Data Channel, bits 2-0 (LVDS Differential signaling)
Y Clock +/-	Primary Data Channel, Clock (LVDS Differential signaling)
Z Data 2-0 +/-	Secondary Data Channel, bits 2-0 (LVDS Differential signaling)
Z Clock +/-	Secondary Data Channel, Clock (LVDS Differential signaling)
VDD	+3.3V Switched Power Supply for LCD display (only powered up when LCD display is active)
Ground	Power Ground, 0V

Connector Part Numbers

J24 plug on CPU board: JST Part Number: BM30B-SRDS-G-TF

Cable-mount socket: JST Part Number: JST SHDR-30V-S-B

4.19 VGA Connector – J25

RED	1	2	R-Ground
GREEN	3	4	G-Ground
BLUE	5	6	B-Ground
HSYNCH	7	8	DDC-Data
VSYNCH	9	10	DDC-Clock

Table 20: J25 – VGA Header Pinout

Signal Name	Definition
RED	RED signal (positive, 0.7Vpp into 75 Ohm load)
R-Ground	Ground return for RED signal

GREEN	GREEN signal (positive, 0.7Vpp into 75 Ohm load)
G-Ground	Ground return for GREEN signal
BLUE	BLUE signal (positive, 0.7Vpp into 75 Ohm load)
B-Ground	Ground return for BLUE signal
DDC-CLOCK/DATA	Digital serial I/O signals used for monitor detection (DDC1 specification)

J25 provides a connection for VGA monitors. Note that while the DDC serial detection pins are present, there is no 5V supply provided (nor are the old "Monitor ID" pins used). Diamond Cable Assembly #**698024** provides a female DB15 connection to interface with a standard RGB monitor.

Connector Part Numbers

J25 Connector on CPU board:	Standard 2x5, 0.1" Box header
J25 Mating Cable Connector:	Standard 2x5, 0.1" female ribbon cable connector

4.20 Video / TV Out Connector – J26

1	S Video - Y
2	S Video - C
3	Composite
4	Ground
5	No-Connect

Table 21: J26 – Video Out Header Pinout

Signal Name	Definition
S-Video "Y"	S-Video "Brightness" (Luminance)
S-Video "C"	S-Video "Color" (Chrominance)
Composite	Composite Video
Ground	Ground (for either S-Video or Composite)
No-Connect	Do not connect this signal; For testing use only

J26 provides a video output for connection to a standard (NTSC) TV. Either S-Video (6-pin mini-DIN) or Composite (RCA Jack) can be used; not both.

Notes:

- Requires Software support to function (Not directly supported in BIOS)
- LCD, S-Video, and Composite are mutually-exclusive: it is not possible to have more than one of these options active at one time.

Connector Part Numbers

J26 Connector on CPU board:	Digi-Key Corp.	640456-5
J26 Mating Cable Connector:	Molex	22-01-3057

4.21 CPU Fan Connector – J27

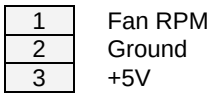


Table 22: J27 – CPU Fan Connector Pinout

Signal Name	Definition
Fan-RPM	TTL signal input that pulses with each revolution of the fan
+5V, Ground	Power Supply for optional CPU Fan (if necessary)

Connector Part Numbers

J27 Connector on CPU board:	Heilind Electronics	89400-0320
J27 Mating Cable Connector:	JST	PHR-3

4.22 LCD Backlight Connector – J28

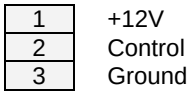


Table 23: J28 – LCD Backlight Connector Pinout

Signal Name	Definition
Control	Output signal (from Hercules-EBX) to allow power-down of backlight
+12V, Ground	Power Supply for LCD Backlight assembly

J28 provides the Backlight power and control for the optional LCD panel. See J24 (above) for details on the LCD data interface. Note that the +12V supply will be removed when the system is powered down; the control signal is to allow the system to power-down the backlight when the system enables monitor-power-down during its power management control.

Connector Part Numbers

J28 Connector on CPU board:	Digi-Key Corp.	A19470
J28 Mating Cable Connector:	Molex	22-01-3037

4.23 Low-Voltage Power Input Connector – J29

1	+Vin
2	+Vin
3	Ground
4	Ground
5	+12V
6	Ground
7	+Vin
8	-12V
9	-5V
10	Power Supply ON

Table 24: J29 – Main Power Input Connector Pinout

Signal Name	Definition
+Vin	Main Input Power (+5V - +28V input range * : see below)
Ground	0-V (Ground) power return path
+12V	Power Supply for in-board 12V devices (including hard drives, auxiliary power, PC/104 power, and LCD Backlight). Range should be 11.9V-13.5V measured at this connector
-12V	Power Supply for PC/104+ -12V devices (no on-board devices)
-5V	Power Supply for PC/104+ -5V devices (no on-board devices)
Power Supply ON	Feedback pin for external ATX supply (when needed) – pulled low when on-board power is inactive

The standard Hercules-EBX Input power is supplied either through J29 from an external mid-range supply. (An option for higher-voltage power supply input may be available).

Hercules-EBX in the standard, mid-range power input configuration supports a voltage range from +4.75V - +28V (with some restrictions). For input voltages from +4.75V to 6V (measured at J29), the function of some 5V devices may be affected due to high-current draw and voltage dips encountered due to these current variations. Specifically:

- Hard Drives attached to the system may not power up correctly and/or may reset;
- Hard Drives, CD-ROMs, and other high-power devices may also draw too much power at these low voltages, causing the system to reset – External power supplies for high-power devices are strongly recommended when the input supply is likely to be this low;
- PS/2 and USB devices may function erratically (or not at all) at low input voltages (an external powered USB hub may alleviate this problem somewhat) – NOTE : this includes USB keyboards, mice, and especially USB boot devices (floppy drives and USB flash drives)
- RS232 range and functionality may suffer;
- Audio Speaker output power may be limited; and
- Data Acquisition accuracy may potentially be slightly affected.

At input voltage ranges above 6V (6V – 28V), these concerns are no longer issues. This main input voltage ("Vin") is used to derive all on-board voltages and power supplies via on-board switching regulators.

The "+12V" power supply input is intended for all on-board (and board-controlled) 12V power supplies, including the PC/104+ 12V supplies, the external hard drive power supply (through J15, described above), and the LCD backlight. If these devices are not to be used, then the "+12V" input may be left unconnected.

Since the PC/104 bus includes pins for -5V and -12V, these voltages may be supplied through J29 if needed (and left unconnected if not needed).

The +5V and +12V voltages are controlled by the ATX power manager switches, while -5V and -12V are routed directly to the corresponding pins on PC/104 bus and are not controlled by the ATX function.

Make sure that the power supply used has enough current capacity to drive your system. The Hercules-EBX requires 12 - 20 Watts or more, depending on what external devices are connected to the board: this could require over 4A on the "+Vin" line (at minimum voltage inputs). In particular, many disk drives need extra current during startup. If your system fails to boot properly, or if disk accesses do not work properly, the first thing to check is the power supply voltage level at J29. Many boot-up problems are caused simply by insufficient voltage due to excess current draw on the "+Vin" supply during thins initialization.

Multiple +5V and Ground pins are provided for extra current carrying capacity if needed. Each pin is rated at 3A max (15W). For the Hercules CPU with a moderate I/O device complement (basic hard drive, key board, mouse, USB devices, and a network PC/104+ card, for instance), 1.4A at +13V is more than sufficient.

ATX control enables the +5V and +12V power to be switched on and off with an external momentary switch. A short press on the switch will turn on power, and holding the switch on for 4 seconds or longer will turn off power (See Utility Header description for J7 above).

Diamond Systems' cable no. **698015** mates with J29. It provides 10 color-coded wires with stripped and tinned leads for connection to user-supplied power sources.

Note that, for cases where the Input Power supply is to be 12V, the "+Vin" and "+12V" input wires may be connected. In this case, be certain that the power supply into the "+12V" does not exceed the voltage requirements for that input pin.

Connector Part Numbers

J29 Connector on CPU board:	Digi-Key Corp.	A1925
J29 Mating Cable Connector:	Molex	22-01-3107

4.24 <OPTIONAL> High-Voltage Power Input Connector – J30

1	Ground
2	+Vwin

Table 25: J30 – Optional High-Voltage Power Input Pinout

Signal Name	Definition
+Vwin	Main Input Power (+13V - +40V input range)
Ground	0-V (Ground) power return path

One board option that may be made available for special, higher-voltage applications is the High-Voltage input. In this case, only the last three pins of J29 would be used (-12 and -5V, if required); otherwise, the main power input would be through this connector. This option is in lieu of the low-voltage power input option (which is standard); this option is not configurable or field-upgradeable. This option is only intended to allow for a higher (and potentially noisier) power supply input than the standard power input provided via J29.

Connector Part Numbers

J30 Connector on CPU board:	Digi-Key Corp.	A1921
J30 Mating Cable Connector:	2-pin female header	

4.25 <OPTIONAL> Compact Flash Slot – J34

An optional Compact Flash Socket may be located under the board, immediately under J17. If this socket is to be used, it will occupy the entire secondary IDE channel. To set the CompactFlash card as an IDE MASTER (so that the BIOS detects it), place a jumper on J5, as detail on page 35.

4.26 <OPTIONAL> Disk-On-Chip – U28 socket

Disk-On-Chip is an optional capability for the system. This option requires customer-specific development: please contact your sales representative for details.

5. JUMPER CONFIGURATION

Refer to the Hercules board drawing on page 9 for locations of the configuration items mentioned here.

5.1 J4: System Configuration

Jumper block J10 is used for configuration of IRQ levels, ATX power control, and CMOS RAM.

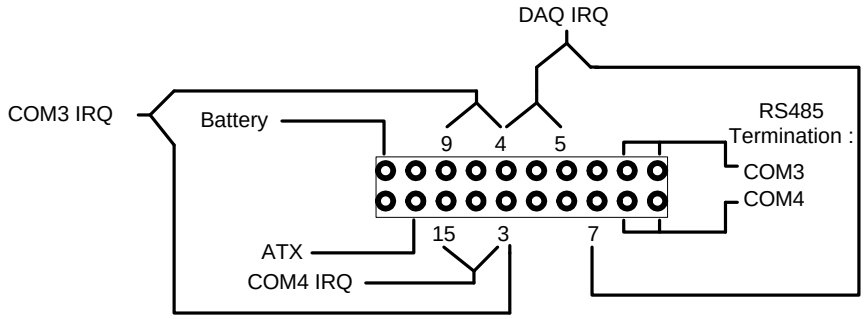


Figure 1 : J4 – System Configuration Header

Serial Port and A/D IRQ Settings

COM3 may be directly set to IRQ3, IRQ4, or IRQ9. COM4 may be directly set to IRQ3 or IRQ15. The A/D circuit (on models that include Data Acquisition) may be set to IRQ4, IRQ5, or IRQ7. It is possible to share an interrupt with an on-board resource (share IRQ3 with COM2, for instance), provided that the OS or driver can handle thee IRQ sharing.

ATX Power Control

The ATX power control is set with this jumper block. If the ATX jumper is out, ATX works normally; an external momentary switch may be used to turn power on and off. A quick contact turns the power on, and a long contact (> 4 seconds) turns the power off. If the ATX jumper is in, the ATX function is bypassed and the system will power up as soon as power is connected.

If the ATX jumper is removed, then the battery-backup for CMOS and Real-time clock settings will no longer function when power is removed.

Erasing CMOS RAM

The CMOS RAM may be cleared by removing a jumper as shown on the next page. This will cause the CPU to power up with the default BIOS settings. To clear the CMOS RAM, power down the CPU, remove the jumper as shown, wait a few seconds, return it to its default position, and then power up again.

Before erasing CMOS RAM, write down any custom BIOS settings you have made!

Default Settings

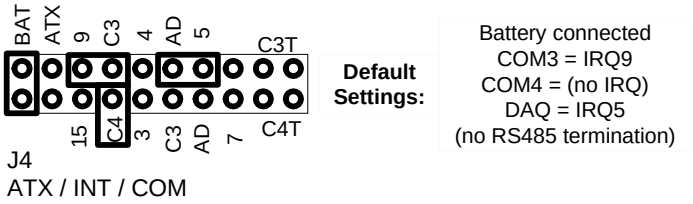


Figure 2 : J4 – Default Jumper Settings

The different configurations for J4 are shown below. Each illustration shows only the jumper of interest. An asterisk (*) indicates the default setting.

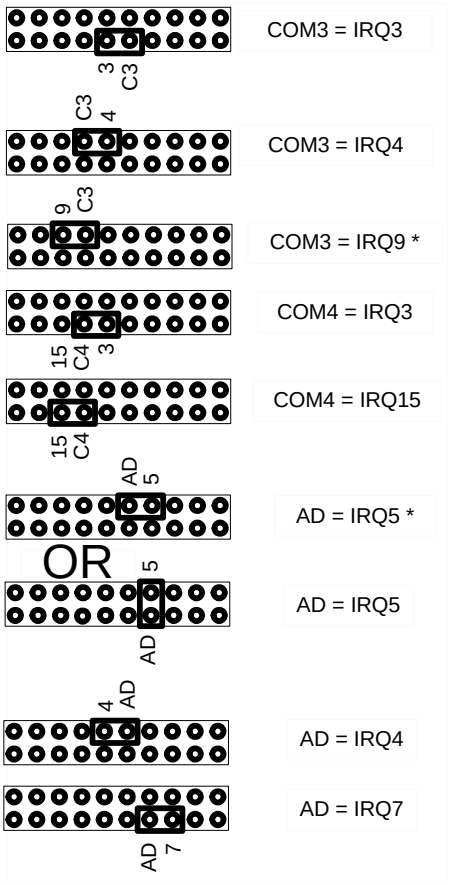


Figure 3 : J4 –IRQ Jumper Setting Examples

Note that COM4 defaults with no hardware IRQ configuration (polling mode only).

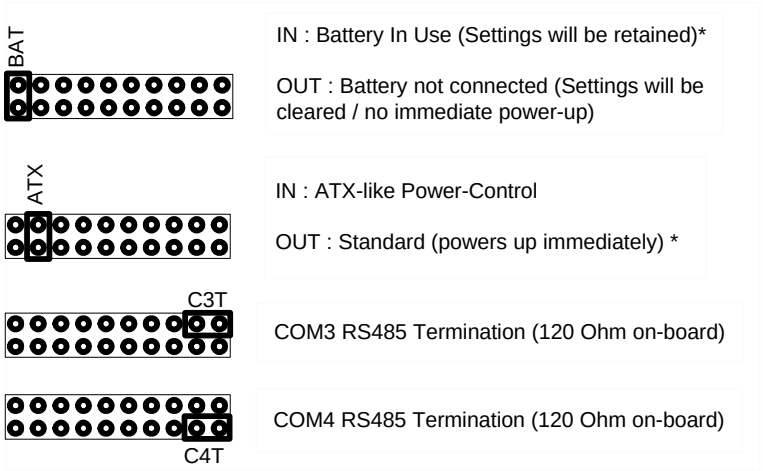


Figure 4 : J4 – Power and Termination Settings

5.2 J5: Data Acquisition Configuration

Jumper block J5 is used for configuration of DIO pull-ups/pull-downs, DIO control signal pull-ups/downs, CompactFlash mode, Flash Write Protect (for boot sector), and COM3/4 Address Selection.

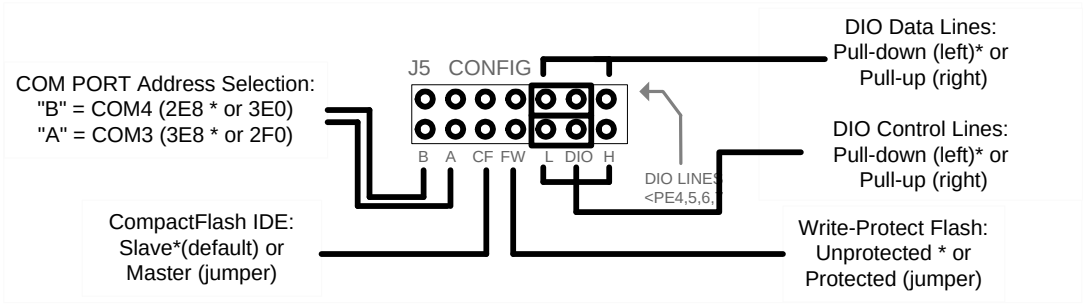


Figure 5 : J5 – Data Acquisition Configuration Header

Serial Port Address Settings

COM3 may be set to either I/O address 0x03E8 (no jumper) or 0x02F8 (jumper added to "A" position on J5). Similarly, COM4 may be set to either I/O address 0x02E8 (no jumper) or 0x03E0 (jumper added to "A" position on J5). These settings are immediately in effect, but the BIOS must start with these jumpers in position in order to automatically detect and configure the ports correctly. Change these settings only while the system is powered down.

CompactFlash IDE Control <OPTIONAL>

The optional CompactFlash slot on the back of the board is configured to the Secondary IDE Channel. As such, it can be detected as either a MASTER device or a SLAVE device. With no jumper, a CompactFlash card would be detected as a SLAVE device. With this jumper, the CompactFlash will be a MASTER IDE Device. Note that a SLAVE device requires a MASTER device on the same IDE channel in order to function.

Write-Protect BIOS Flash

Adding this jumper forces protection of the boot-sector of the Compact Flash. This allows for dynamic Crisis Recovery in the case where the BIOS PROM becomes corrupted. Note that this option may not be user-selectable – write Protection may be enforced regardless of this jumper selection.

DIO Pull-up / Pull-Down Selections

The Digital I/O lines in the Data Acquisition section are broken into two blocks: General Purpose DIO lines (DIO channels A-D, and Channel E bits 3-0), and Multiplexed Control lines (DIO Channel E bits 7-4).

The top three pins allow for a pull-down (left) or pull-up (right) selection for the General-Purpose pins. The bottom three pins allow a similar selection for the multiplexed control lines. This allows these alternate-function pins to be selected separately since their function may require a different default state than that provided to the standard digital I/O lines.

Default Settings

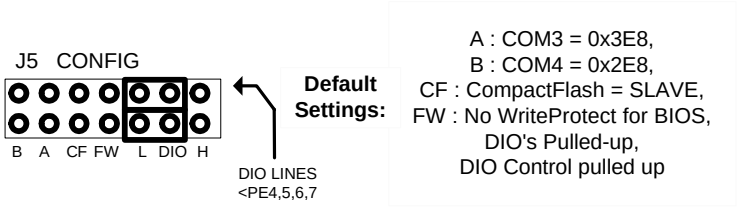


Figure 6 : J5 – Default Jumper Settings

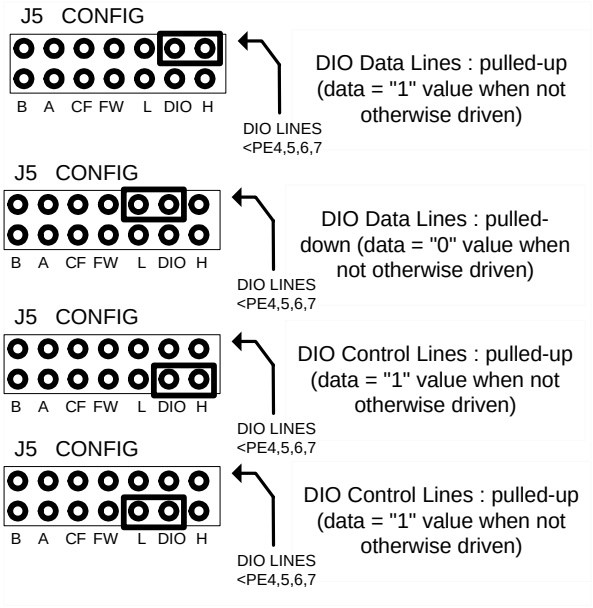


Figure 7 : J5 – DIO Pull-up/Pull-Down Examples

5.3 J19 : PCI VI/O Voltage Setting

J19 provides simple access to the VIO setting for PC/104+ cards. This setting sets the voltage supplied on the "VIO" power pins of the PC/104+ connector (J3). Note that the "VIO" voltage is used on most cards to supply the I/O Voltage for all PCI signals.

The Hercules-EBX can support either I/O voltage range (all on-board signals are driven from 3.3V power rails, but are 5V tolerant), so the determination of the I/O voltage is entirely dependant on the types of PC/104+ cards plugged in.

1	+5V
2	PCI VIO
3	+3.3V

Table 26: J19 – PC/104+ (PCI) VIO Power Selection

Signal Name	Definition
+5V	Main +5V Power supply on Hercules-EBX board
+3.3V	Main +3.3V Power supply on Hercules-EBX board
PCI VIO	"V I/O" pins on J3

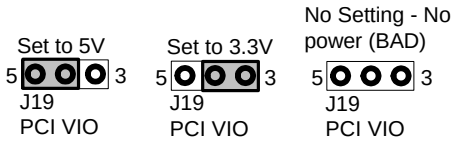


Figure 8 : Possible VIO Settings for J19

PC/104+ cards are supposed to be keyed to identify the correct voltage setting – no key is supposed to mean that the card is universal and can accept either power setting. There are essentially 4 possibilities:

1) Card keyed for 5V
2) Card keyed for 3.3V
3) Card not keyed – universal (can operate with either voltage setting)
4) Card incorrectly keyed or not keyed but with certain requirements

The first three possibilities can be easily determined by checking the keying of the card:

- 5V card = Pin A1 missing / pin D30 present
- 3.3V Card = Pin A1 present / pin D30 missing
- Universal Card = both pins present

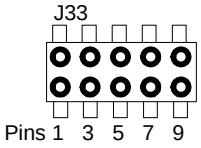
The only solution for cards that are incorrectly keyed is to read the documentation and verify the I/O voltage (if it is called out in the card description). While not a widespread issue, this is something to be aware of when starting to work with a new PC/104+ card.

See pages 12 and 119 for details on the PC/104+ Connector and PC/104+ cards. Note that this voltage selection is not used for standard PC/104 cards; only the PCI-signaling of PC/104+.

5.4 J33: Data Acquisition Calibration Test Points

Jumper block J33 is used for measuring internal Analog Data Acquisition voltages to ensure precise calibration. For most applications, these test points will not be of use.

If you require access to these internal voltages, here is a listing of the signals present on this header:



AD IN (+)	1	2	Ground
AD VIN	3	4	UNIADJ
+5V (ADC power)	5	6	-5V Reference
+15V (ADC Power)	7	8	+ Dref Voltage
-15V (ADC Power)	9	10	- Dref Voltage

Table 27: J33 – DAQ Test Point Pinout

5.5 CRISIS RECOVERY: System Recovery Contacts

Just below J18 is a small square labeled “Crisis Recovery” which encircles two metal pads on the PCB. If these two pads are briefly shorted before and during power-up, the system will be forced into a System Recovery mode. This mode forces the system to re-load the BIOS code from a floppy disk and overwrite the current on-board BIOS (useful in cases where a BIOS update is required or when BIOS corruption is suspected).

Failsafe mode operation is described on page 43.

6. SYSTEM FEATURES

6.1 System Resources

The table below lists the default system resources utilized by the circuits on Hercules-EBX.

Device	Address (Hex)	ISA IRQ	ISA DMA
Serial Port COM1	I/O 3F8-3FF	4	-
Serial Port COM2	I/O 2F8 – 2FF	3	-
Serial Port COM3	I/O 3E8 – 3EF	9	-
Serial Port COM4	I/O 2E8 – 2EF	N/C*	-
IDE Controller A	I/O 1F0 – 1F7	14	-
IDE Controller B	I/O 170 - 177	15	-
A/D Circuit (when applicable)	I/O 240 – 25F	5	-
Serial Port / FPGA Control	I/O A50-A5F	-	-
Ethernet	OS-dependant	OS-dependant	-
USB	OS-dependant	OS-dependant	-
Sound	OS-dependant	OS-dependant	-
Video	OS-dependant	OS-dependant	-

Table 28: System Resources

* = COM 4 is not connected to an IRQ by default. To use COM4 on the default jumper pinout, either COM1 must be disabled/changed (for access to IRQ3) or the Secondary IDE controller must be disabled (for access to IRQ15). Alternatively another IRQ may be used, but a wire would be required : COM4 only jumpers directly to either IRQ15 or IRQ3.

Note that most of these resources are configurable and, in many cases, the Operating System will alter these settings. The main devices that are subject to this dynamic configuration are on-board Ethernet, sound, video, USB, and any PC/104+ cards that are in the system. These settings may also vary depending on what other devices are present in the system : Adding a PC/104+ card may cause the on-board Ethernet resources to change, for instance.

The Serial Port settings for COM3 and COM4 are jumper selectable whereas the settings for COM1 and COM2 are entirely software-configured in the BIOS.

6.2 COM Port / FPGA Control Registers

A set of registers is located at Address 0xA50-0xA5F for the purposes of controlling the enhanced Serial Port features, as well as some FPGA control capability. Only two registers from this range should be accessed by the user:

Address	Bit	Read - Write	Functional Description
0xA50	0	Read-Only	COM3 Address Selection (read from J5 – "A")
	1	Read-Only	COM4 Address Selection (read from J5 – "B")
	7-2	Read-Only	Unused
0xA51	0	Read / Write	COM3 Enable (1) / Disable (0)
	1	Read / Write	COM3 : 0 = RS232 1 = RS485
	2	Read / Write	COM4 Enable (1) / Disable (0)
	3	Read / Write	COM4 : 0 = RS232 1 = RS485
	7-4	Read / Write	Unused (set to 0)
0xA52-0xA5F	7-0	-	Reserved – do not access

Table 29: I/O COM3/4 Control Register Definition

6.3 Console Redirection to a Serial Port

In many applications without a video card it may be necessary to obtain keyboard and monitor access to the CPU for configuration, file transfer, or other operations. Hercules-EBX supports this operation by enabling keyboard input and character output onto a serial port (console redirection). A serial port on another PC can be connected to the serial port on Hercules-EBX with a null modem cable, and a terminal emulation program (such as HyperTerminal) can be used to establish the connection. The terminal program must be capable of transmitting special characters including F2 (some programs or configurations trap special characters).

The default Hercules-EBX BIOS setting enables console redirection onto COM2 during POST (power on self-test). The communication parameters are 115.2Kbaud, N, 8, 1. When the CPU is powered up, the BIOS will output POST information to COM2 and monitor it for any keyboard activity. You can enter the BIOS by pressing F2 during this time. In the default configuration, after POST is finished and the CPU boots, console redirection is disabled.

There are three possible configurations for console redirection:

- POST only (default)
- Always On
- Disabled

To modify the console redirection settings, enter the BIOS, select the Advanced menu, and then select Console Redirection. In Com Port Address, select Disabled to disable the function, On-board COM A for COM1, or On-board COM B for COM2 (default).

If you select Disabled, you will not be able to enter BIOS again during power-up through the serial port. To reenter BIOS when console redirection is disabled, you must either install a PC/104 video

board and use a keyboard and terminal or erase the CMOS RAM, which will return the BIOS to its default settings. CMOS RAM may be erased by moving a jumper. See page 33 for instructions.

Before erasing CMOS RAM, write down any custom BIOS settings you have made!

If you erase the CMOS RAM, the next time the CPU powers up COM2 will return to the default settings of 115.2Kbaud, N, 8, 1 and operate only during POST.

If you selected COMA or COMB, then continue with the configuration:

For Console Type select PC ANSI. You can modify the baud rate and flow control here if desired.

At the bottom, for Continue C.R. after POST, select Off (default) to turn off after POST or select On to remain on always.

Exit the BIOS and save your settings.

6.4 Watchdog Timer

Hercules-EBX contains a watchdog timer circuit consisting of two programmable timers, WD1 and WD2, cascaded together. The input to the circuit is WDI, and the output is WDO. Both signals appear on Digital I/O connector J8. WDI may be triggered in hardware or in software. A special “early” version of WDO may be output on the WDO pin. When this signal is connected to WDI, the watchdog circuit will be retriggered automatically. A block diagram is provided here:

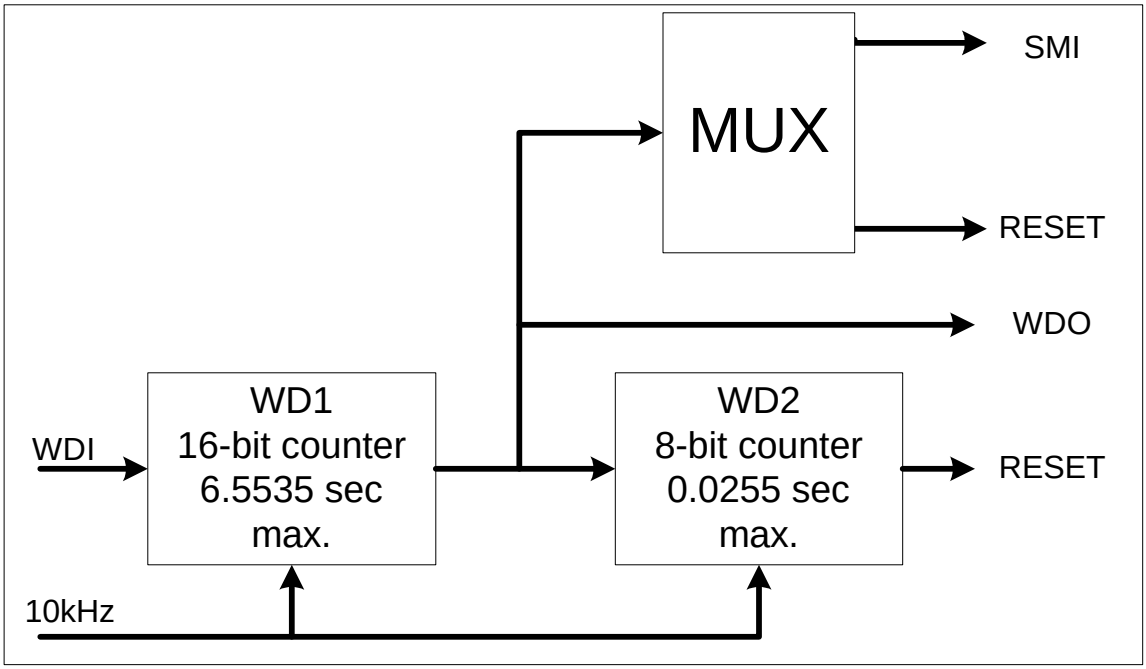


Figure 9 : Watchdog Timer Block Diagram

The duration of each timer is user-programmable. When WD1 is triggered, it begins to count down. When it reaches zero, it triggers WD2, sets WDO high, and may also generate a user-selectable combination of these events:

- System Management interrupt (SMI)
- Hardware reset

WD2 then begins to count down. When WD2 counter reaches zero, it will unconditionally cause a hardware reset. The WD2 timer is provided to give external circuits time to respond to the WDO event before the hardware reset occurs.

The watchdog timer circuit is programmed via I/O registers located on Page 0: Base +28-31 Detailed programming can be found on page. The Hercules-EBX watchdog timer is supported in the DSC Universal Driver software version 5.7 and later.

6.5 Failsafe Mode / BIOS Recovery

The Hercules-EBX board is provided with the capability to force the BIOS code to be updated on power-up. The Hercules-EBX will always check the BIOS for errors upon power-up (based on an internal CRC code) and may try to force an update in this case.

Otherwise, the BIOS can be forced to update by shorting the two "CRISIS RECOVERY" pads located just below J18 (the serial port header). If these pins are shorted as the board powers-up and enters the self-test, it will immediately search for a USB floppy device on any of the 4 USB ports. Once a drive is found, it will immediately search for a special "Crisis Recovery" disk (provided by Diamond Systems). If the correct data is found, then the board will immediately begin loading and updating the code.

To force the BIOS to re-program the code, short the two "Crisis Recovery" pins together and, with a USB floppy drive connected and a Crisis Recovery disk in the drive, power-up the system. After the system powers up and the floppy drive is accessed, the two pins should be released – if the two "crisis Recovery" pins are shorted at the conclusion of the update, the system will reboot and restart Crisis Recovery.

Once Crisis Recovery has started with a valid Floppy drive, do not turn off the system until the system reboots itself and comes up to the POST screen.

See the information in the \Utilities\BIOS Recovery folder of the Hercules-EBX files area of the DSC customer CD for instructions on using this program.

Note that the onboard settings should always be reloaded within the BIOS setup screens anytime the BIOS is updated – even if it is reprogrammed with the same BIOS code. CMOS settings that are not reloaded with defaults may cause unexpected system behavior – in short, ALWAYS go into the BIOS menus and "load defaults" as soon as Crisis Recovery completes. Once defaults are loaded, alternative settings may be entered and saved.

6.6 Flash Memory

Hercules-EBX contains a 2Mbyte 16-bit wide flash memory chip for storage of BIOS and other system configuration data.

6.7 Backup Battery

Hercules-EBX contains an integrated RTC / CMOS RAM backup battery. The battery is located adjacent to the PC/104 bus connector J1 (within the PC/104 outline). This battery has a capacity of 120mAH and will last over 3 years in power-off state. Note that there are two connection points for alternative, external battery power sources:

- Utility Header(J7) – pins 12 (V+) and 14 (ground);
- External Battery Header (J20)

The external battery should be 3-3.6V and should be able to provide a continuous supply with a nominal 2uA continuous current drain and a peak short-term drain of 1mA. An external battery is only recommended where concern for on-board CMOS settings and/or time accuracy make such redundancy worthwhile.

The on-board battery is activated for the first time during initial factory configuration and test.

6.8 System Reset

Hercules-EBX contains a chip to control system reset operation. Reset will occur under the following conditions:

- User causes reset with a ground contact on the Reset input
- Input voltage drops below 4.75V
- Over current condition on output power line

The ISA Reset signal is an active high pulse with a duration of 200ms. The PCI Reset is active low, with a pulse width duration of 200 msec typical.

6.9 On-Board Video

The on-board video for the Hercules-EBX board is based on an S3-TwisterT (VIA 8606 "PN133T" Northbridge) video system. As such, the board memory is shared between the Video and main system memory. A block of memory is configured (via BIOS Settings, accessible in the BIOS configuration menus) for video which is then removed from use for main system memory. This implies that the more memory used for the Video, the less memory is available for system resources.

Note that the video memory can be set at 8Mbytes for almost all applications – increasing the memory size will not increase video performance. Additional memory will only benefit the limited 3D support provided by the chipset. Also note that 3D hardware acceleration is not supported across extended temperature range. In general, this 3D hardware is typically only used for 3D games – most likely, these limitations will not affect most embedded applications.

Note that the low-level BIOS can support LCD output in conjunction with standard RGB output (i.e., dual-displays). Similar support for TV output is limited to the OS: the BIOS itself does not directly support the TV Out functionality.

7. BIOS

7.1 BIOS Settings

Hercules-EBX uses a BIOS from Phoenix Technologies modified to support the custom features of the Hercules-EBX board. Some of these features are described here.

To enter the BIOS during system startup (POST – power on self-test), press F2.

Serial Ports

-The address and interrupt settings for serial ports COM1 – COM4 may be modified. COM1 and COM2 address and interrupt settings are done in the BIOS, Advanced menu, I/O Device Configuration. See page 50 for details.

-The addresses of COM3 and COM4 are configurable on the board via J5. These selections are detected in the BIOS automatically. The IRQ selections for COM3 and COM4 are configured on J4. These selections are not automatically detected and must be manually configured to match the jumper settings for the two COM ports.

Select Advanced menu, Advanced Chipset Control, I/O Chip Device Configuration. See page 47 for details.

IDE Settings

The IDE controller provides two separate IDE channels:

- PRIMARY IDE – this IDE Channel is available via J16 (44-pin laptop-type IDE connector).
- SECONDARY IDE – This IDE Channel is available via J17 (40-pin, standard UDMA connector)

Be aware of which channel is which if you are attempting to disable one unused channel in order to free up IRQ resources.

“32-bit I/O” settings can be manually activated for each drive. Note that this setting only affects low-level BIOS accesses to the drives when using BIOS system calls (typically under DOS) and may cause system instability for OSes or applications that do not support these types of accesses. For general operation, this will not grant a noticeable performance boost: the setting should be left “disabled” unless absolutely necessary.

LCD Video Settings

The Hercules-EBX provides direct digital support for LVDS-based LCD interfaces only. As such, there are two settings that affect this support during BIOS boot:

- Boot Video Device – By default, this is set to “AUTO”. With the AUTO setting, the system will attempt to identify an RGB monitor (via DDC) and, if no RGB monitor is detected then the system enables LCD support. If you wish to use the LCD display regardless of standard monitor connection (i.e., with both connected at once), then set “Boot Video Device” to “Both”.
- Panel Type – This setting defaults to “7”. Do not alter this setting unless specifically instructed to do so. This setting affects the LCD display modes supported; mode “7” is the only setting currently supported.

Miscellaneous

-Memory Cache Settings:

Unless there is a specific reason to change these settings, it is best to keep these settings as-is. Certain system functions (such as USB keyboard support under BIOS menus) may be adversely affected by changes to these settings, due mainly to a heavy reduction in performance. These cache settings can make a huge difference for low-level BIOS calls and, as such, can severely limit performance if they are disabled.

-On the Advanced Chipset Control screen, the following settings should be retained:

Frame Buffer Size: 8MB

AGP Rate: 4X

Expansion Bus Performance: Normal

The Frame Buffer size can be increased for specific applications; just be aware that an increase in this memory size will result in a decrease in overall system memory available. The AGP rate affects internal video accesses and does not affect any external bus speeds.

"Expansion Bus Performance" is an adjustment to allow an increase in ISA I/O Access speeds. For applications where ISA I/O accesses seem to be a limiting factor, this performance may be increased to "Accelerated". Be aware that increasing these timings may adversely affect system stability with external add-on PC/104 cards. This setting has no direct affect on PCI or memory speeds; it only affects ISA PC/104 devices. It is best to leave this setting at "Normal" if there are no ISA I/O Performance issues.

-On the Advanced screen, the following settings should be retained:

Installed O/S	Win98
Large Disk Access Mode	DOS

-On the On-Chip Multifunction Device screen, the following settings should be retained:

USB Device	Enabled
Legacy Audio	Disabled

"Legacy Audio" will only affect DOS-based applications when used with the VIA-supported DOS Drivers. Enabling this setting will require system I/O, IRQ, and DMA resources. It is strongly recommended that this setting be left "Disabled."

-On the PCI and ISA Configuration pages (from the Advanced screen), the following setting should be retained:

PCI IRQ Level 1-4	Autoselect for all
PCI/PNP ISA UMB Region Exclusion	Available for all

-The Power Management Screen will only be in effect when under DOS. Otherwise, the OS power management settings will pre-empt these settings. The only power management mode supported by the system is "Power-On Suspend" – other suspend modes are not supported and should not be used under any OS (Examples of unsupported suspend modes: "Hibernate" under Windows and "Suspend-to-Disk" or "Suspend-to-RAM".)

- The Memory Shadow page of BIOS options should not be modified unless you are certain what you are doing. These settings can adversely affect system performance and, potentially, system reliability.

7.2 BIOS Download / Crisis Recovery

Because the BIOS is stored in reprogrammable Flash memory, it is possible that the BIOS could be accidentally erased when trying to write other files into the Flash. To recover from this situation the CPU chip on Hercules-EBX contains a special failsafe section of ROM code that can be activated on power-up. A Diamond Systems software utility is provided to enable system recovery by downloading the BIOS to the flash memory through a USB floppy drive when the CPU is booted up to the BUR.

Typically, this "Crisis Recovery" Process is initiated by shorting the "Crisis Recovery" pads on the main board (located just under J18) while powering up the unit. If the board is mounted in such a manner that these pins are not readily accessible, then Crisis Recovery should be initiated by shorting RTS to RI on COM1.

The Sequence for Crisis Recovery is as follows:

1) **Short "Crisis Recovery" pads or RTS – RI on COM1**
2) **Connect USB Floppy Drive with Crisis Recovery floppy disk inserted**
3) **Power-up / reset system**
4) **Floppy disk should be accessed (light on floppy drive starts up and floppy whirs for several seconds); if you have a PC speaker attached to the utility header, after a few seconds you should hear some beeps**
5) **Unshort the "Crisis Recovery pads or the RTS-RI connection after the Crisis Recovery starts (i.e., after the floppy is first accessed or after the first system beep)**
6) **At the conclusion of the Crisis Recovery BIOS update, the system will beep and reset**
7) **Immediately go into the BIOS setup screen (F2 from initial BIOS POST screen) and press F9 to load defaults.**
8) **While in the BIOS setup menus, re-set any non-default settings that you require**
9) **Exit the BIOS menus and save the settings**

PC Serial Port Crisis Recovery (DE-9)
7 (RTS)
9 (RI)

Table 30: Crisis Recovery Loopback

Contact Diamond Systems technical support for further assistance.

7.3 BIOS COM Port Settings

The BIOS allows for configuration of the four COM PORTs. Note that the COM PORT configuration is handled slightly differently for COM PORTs 1 & 2 versus COM PORTs 3 & 4.

COM PORTs 1&2 are both located inside the core chipset used for the Hercules-EBX. As such, the configuration procedures for these two COM PORTs are more limited, but are fully-configurable in software (via BIOS Set-up Screens).

- COM 1 has the following options:
    - ISA I/O Address : 0x3F8 (default), 0x2F8, 0x3E8, or 0x2E8
    - ISA IRQ : IRQ4 (default) or IRQ3

- COM 2 has the following options:
    - ISA I/O Address : 0x2F8 (default), 0x3F8, 0x3E8, or 0x2E8
    - ISA IRQ : IRQ3 (default) or IRQ4
    - Mode : Normal (default), IrDA, ASK_IR
        - Note that the two IR modes require an external IR transceiver, connected to the two IR I/O pins located on the Utility Header (J7). See page 14 for connection details.

COM PORTs 3&4 are handled by an external UART (XR16C2850). As such, the configuration is handled a bit differently. The I/O Addresses are not configurable in software; rather they are determined based on the jumper settings from J5: Add or remove a jumper from header location "A" to change COM 3 address or location "B" to change COM 4 address. Note that the BIOS detects these I/O settings and configures COM3 and COM4 I/O Addresses accordingly.

The IRQ's for the two COM parts are manually selectable via jumpers on header J4 (see page 34 for details of IRQ selection). These settings must then be manually entered into the BIOS in order for these IRQ's to be properly configured and reported from the BIOS to the operating system.

The Setting for RS-232 versus RS-485 modes for COM PORTs 3 & 4 is software-selectable in the BIOS.

- COM 3 has the following options:
    - ISA I/O Address:
        - J5 "A" Header location with no jumper = COM 3 has I/O Address 0x3E8
        - J5 "A" Header location with jumper = COM 3 has I/O Address 0x2F0
    - ISA IRQ :
        - Jumper settings : IRQ 3, IRQ 4 (default), or IRQ 9
    - Mode:
        - RS-232 (Default) or RS-485

- COM 4 has the following options:
    - ISA I/O Address:
        - J5 "B" Header location with no jumper = COM 3 has I/O Address 0x2E8
        - J5 "B" Header location with jumper = COM 3 has I/O Address 0x3F0
    - ISA IRQ :
        - Jumper settings : IRQ 3 (Default), IRQ 15
    - Mode:
        - RS-232 (Default) or RS-485

7.4 BIOS Console Redirection Settings

For applications where the Video interfaces will not be used, the textual feedback typically sent to the monitor can be redirected to a COM PORT. In this manner, a system can be managed and booted without the need for any video connection.

The BIOS allows the following configuration options for Console Redirection to a COM PORT:

- COM PORT Address : Disabled (default), COM PORT A, or COM PORT B
    - NOTE: **IF Console Redirection is enabled here, note that the Associated COM PORT ("A" here referring to COM 1 and "B" referring to COM 2) will be enabled, regardless of the COM PORT settings elsewhere.**
- "Continue CR After POST" : Off (default) or On
    - Determines whether the system is to Wait for CR over COM PORT before continuing (after POST is completed, before OS starts loading)
- Baud Rate : 19.2K (default), 300, 1200, 2400, 9600, 38.4K, 57.6K, 115.2K
- Console Connection : Direct (default) or Modem
- Console Type : PC ANSI (default, VT100, VT100 (8-bit), PC-ANSI (7-bit), VT100+, or VT-UTF8
- Flow Control : CTS/RTS (default), XON-XOFF, None
- # of video Pages to support 1(default) to 8

Note that Console Redirection only works for text-based interaction. If the OS enables video and starts using direct video functions (as would be the case with a Linux X-terminal or Windows, for instance), then Console Redirection will have no effect and video would be required.

8. SYSTEM I/O

8.1 Ethernet

Hercules-EBX includes a 10/100Mbps Ethernet connection using Cat-5 (100BaseT) wiring. The signals are provided on two connectors: a vertical RJ45 connection (J10) or 6-pin header (J11) on the right edge of the board.

For applications where the on-board RJ45 might be inaccessibly or inconvenient, Diamond Systems' cable no. **698002** mates with the header and provides a standard RJ-45 connector in panel-mount form for connecting to standard Cat5 network cables.

1	Common
2	RX-
3	Common
4	RX+
5	TX-
6	TX+

Table 31: J11 – Ethernet Connector

The Ethernet chip is the National Semiconductor DP83815 MacPhyter chip. It is connected to the system via the board's internal PCI bus.

The Hercules-EBX Software CD includes Ethernet drivers for Windows 95, Windows 98, Windows NT, and Linux. The latest drivers can also be downloaded from National Semiconductor's website at www.national.com. Search for DP83815 to reach the product folder.

A DOS utility program is provided for testing the chip and accessing the configuration EEPROM. Each board is factory-configured for a unique MAC address using this program. To run the program, you must boot the computer to DOS. The program will not run properly in a DOS window inside of Windows. In normal operation this program should not be required.

Additional software support includes a packet driver with software to allow a full TCP/IP implementation.

8.2 Serial Ports

Hercules-EBX contains 4 serial ports. Each port is capable of transmitting at speeds of up to 115.2Kbaud. Ports COM1 and COM2 are built into the standard chipset. They consist of standard 16550 type UARTs with 16-byte FIFOs.

Ports COM3 and COM4 are derived from an Exar 16C2850 dual UART chip and include 128-byte FIFOs. Ports 3 and 4 may be operated at speeds up to 1.5Mbaud with installation of high-speed drivers as a custom option.

The serial ports use the following default system resources:

Port	Address range	IRQ
COM1	I/O 3F8 – 3FF	4
COM2	I/O 2F8 – 2FF	3
COM3	I/O 3E8 – 3EF	4
COM4	I/O 2E8 – 2EF	3

Table 32: COM PORT Default Resource Listing

The settings of COM1 and COM2 may be changed in the system BIOS. Select the Advanced menu, then I/O Device Configuration. The base address and interrupt level may be modified on this page.

The settings of COM3 and COM4 may be changed using a different procedure:

The addresses of these two ports are selected with jumpers on J5 – these settings are autodetected by the BIOS based on this jumper setting. Each COM port has only two options: one default address (no jumper) and one alternate address (with jumper).

The interrupt (IRQ) settings for COM3 and COM4 are selected with J4. COM3 may use IRQ4 or IRQ9. COM4 may use IRQ3 or IRQ15. See page 34 for serial port IRQ jumper settings. Note that once these jumper selections are made, the user must update the Serial Port IRQ settings to match these selections – the IRQ settings are NOT autodetected in the same manner that the address settings are.

8.2.1 RS-232 MODE

RS-232 mode is the standard mode for most PC applications. COM1 and COM2 are always RS232-only (there is a possible product option for RS485-only instead). COM3 and COM4 are RS-232 by default - the settings are managed in the BIOS under the "I/O Device Configuration" menu.

RS232 mode for all 4 ports provides complete signaling support, including all handshaking signals as well as the RI or "Ring Indicate" signal.

8.2.2 RS-485 MODE

COM3 and COM4 are independently selectable between RS232 mode (default) and RS485 mode. If RS485 mode is chosen, then special consideration is required to implement RS485 mode in both hardware and software.

In hardware, the critical issues for RS485 mode are:

1) No handshaking lines are supported – receive and transmit only,
2) Differential signaling – two wires each (high and low) for receive and transmit, and
3) Signal definitions for J18 change depending on the mode for each serial port

See page 24 for details of RS-232 versus RS-485 pinouts on connector J18.

In software, the control of the RS485 Transmit is handled via the serial port RTS signal: a handshaking signal for RS232, it is used as a write-control signal for RS-485 operation.

The RS-485 implementation for COM Ports 3&4 always receives the data being sent. For example, when data is transmitted from COM Port 3, the same data will be locally echoed back into the receive buffer of COM Port 3. This allows for data verification in order to identify RS-485 network collisions (i.e., if another device sends data onto the RS-485 wires at the same time, the data coming into the receive buffer will not match or will not be received at all).

To transmit data for one of these RS-485 ports, the RTS signal must be driven active to transmit. As soon as this setting is made, the transmitter for that RS485 port is active and will remain so until the RTS signal is returned to its default (no-transmit) state.

The typical sequence to transmit data on a shared RS-485 cable is the following:

1) Set RTS high (enable transmit)
2) Send data, which will be echoed to the receive buffer of the same port
3) Set RTS low (disable transmit)
4) Verify that data is received and that it matches the transmit data; if not, re-transmit

8.3 PS/2 Ports

Hercules-EBX supports 2 PS/2 ports: one dedicated for keyboard and the other dedicated for mouse function. The two PS/2 ports are accessible via a cable assembly (DSC#**698022**) attached to J6. Support for these ports is independent of, and in addition to, mouse and keyboard support via the USB ports.

8.4 USB Ports

Hercules-EBX contains 4 USB Ports (referenced as “USB0” through “USB3”). All four USB ports are accessible via cable assemblies attached to J22 (“USB0” and “USB1”) and J21 (“USB2” and “USB3”). One of these ports, “USB1”, is also available via on onboard vertical USB connector J23, located on the top-left corner of the board. J23 should only be used when “USB1” on J22 is not used – do not connect USB devices into both connectors or neither device will function.

USB support is intended primarily for the following devices (although any USB1.1-standard device should function without issue):

- Keyboards
- Mice
- USB Floppy Drive (NOTE : this is required for “Crisis Recovery” of boot ROM)
- USB flash disks

The BIOS fully supports the USB keyboard during BIOS initialization screens, as well as legacy emulation for DOS-based applications.

The USB ports can be used for keyboards and mice at the same time that the PS/2 keyboard and mouse are plugged in – multiple devices of the same type are supported, although this can obviously get rather confusing.

9. NOTES ON OPERATING SYSTEMS AND BOOTING PROCEDURES

9.1 Windows Operating Systems Installation Issues

Installation of Windows operating systems (Win98/2000/XP) should follow the sequence below. If the sequence is not followed certain drivers might not work and may prevent the device from functioning properly under Windows.

1) Enable CD-ROM support in the BIOS. Change boot sequence in BIOS so system boots from CD-ROM first.
2) Insert Windows installation CD into CD-ROM and restart computer
3) Follow the instructions for installing Windows.

9.1.1 DRIVER INSTALLATION

4) Install the Via "4-in-1" driver first. Install driver v4.35 for Windows 98, v4.40 or later for Windows 2000/XP. During installation select the following options:
   a. Normal Install
   b. Select the following four options
      i. VIA ATAPI Vendor Support Driver
      ii. AGP VxD Driver
      iii. IRQ Routing Miniport Driver
      iv. VIA INF Driver v1.40a
   c. Install VIA ATAPI Vendor Support Driver
   d. Enable DMA Mode
   e. Install VIA AGP VXD in Turbo Mode
   f. Install VIA IRQ Routing Miniport Driver
5) Now install the Via/S3 Video driver. Follow installation instructions.
6) Install the Via Sound driver. Make sure the sound driver is ComboAudio v3.90 or later
7) Install the National Semiconductors Network driver.
8) The USB driver for the floppy drive needs to be loaded before the USB floppy drive will be functional under Windows (legacy support will provide floppy access for DOS boot).

9.1.2 BIOS SETTINGS FOR WINDOWS

- "OS" Setting : When using any version of Windows, the "Operating System" selection in the BIOS setup menus should be set to "Win98".
- "Audio" Setting : "Legacy Audio" must be disabled for Windows to boot properly.

9.1.3 COMPACTFLASH UNDER WINDOWS

CompactFlash is not directly supported by Windows 98. A special driver may be available - – see the vendor of your specific CompactFlash card for details. Without special drivers, Windows 98 will not recognize the CompactFlash at all.

CompactFlash support is automatic under Windows 2000 and XP.

9.2 DOS Operating Systems Installation Issues

Installation of DOS operating systems (MS-DOS, FreeDOS, ROM-DOS) should follow the sequence below.

1) Enable the following in BIOS:
   a. Floppy Drive detection.
   b. Legacy USB support.

2) Change BIOS boot sequence so system boots through USB floppy drive.
3) Insert DOS installation floppy disk into USB floppy drive and start/restart system.
4) Install various drivers needed.

Note : For DOS Ethernet to work, in BIOS set “Operating System” to “other”. DOS Sound emulation currently is not functional.

9.3 CompactFlash Compatability Issues under DOS

Compact flash has some incompatabilities with certain utilities under various flavors of DOS:

1) Compact Flash with ROM-DOS

ROM-DOS FDISK utility does NOT work with Compact Flash drives. ROM-DOS FORMAT and SYS do work. If compact flash already has a DOS partition, then ROM-DOS utilities can be used to FORMAT the compact flash and install operating system files on to compact flash.

2) Compact Flash with FreeDOS

FreeDOS FDISK or FORMAT utility do not work with compact flash. The FreeDOS SYS utility is functional with CompactFlash.

3) Compact Flash with MS-DOS

MS-DOS FDISK, FORMAT, and SYS utilities are not functional when used with CompactFlash. MS-DOS operating system files can not be installed on to compact flash.

10. DATA ACQUISITION CIRCUIT

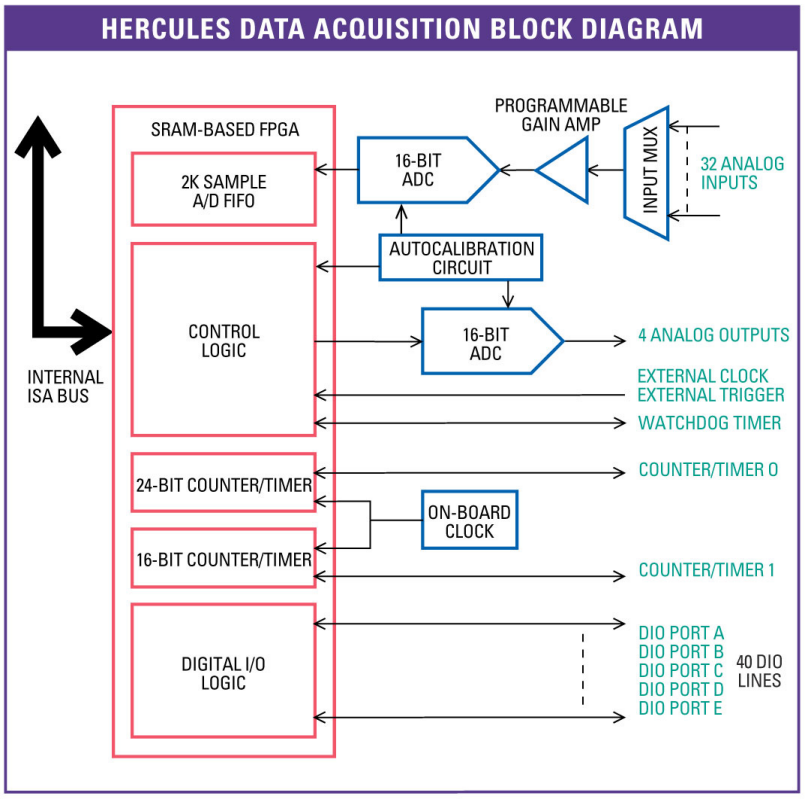
Hercules-EBX Models with Data Acquisition contain a data acquisition subsystem consisting of A/D, D/A, digital I/O, and counter/timer features. This subsystem is equivalent to a complete add-on data acquisition module.

The A/D section includes a 16-bit A/D converter, 32 input channels, and a 2048-sample (4kByte) FIFO. Input ranges are programmable, and the maximum sampling rate is 250 KHz. The D/A section includes 4 12-bit D/A channels. The digital I/O section includes 40 lines with programmable direction. The counter/timer section includes a 24-bit counter/timer to control A/D sampling rates and a 16-bit counter/timer for user applications. A 4-channel PWM controller is built in to provide a method to automatically generate PWM-based waveforms.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store a user-selected number of samples, and the interrupt occurs when the FIFO reaches this threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate. In DOS or similar low-overhead operating systems the circuit can operate at sampling rates of up to 250 KHz.

Note that the interrupt rate when using high sample-rates is kept low due to the large FIFO buffer. With a 250 kHz sampling rate and a FIFO threshold of 1024 samples (half-full), the interrupt rate is kept to a reasonable range of roughly 250Hz. Reducing the FIFO interrupt threshold will increase the interrupt rate for a given sampling frequency, while increasing the threshold (especially to FIFO full) will increase the risk that samples might be lost due to interrupt latency. This rate will be an issue under multitasking OSes such as Windows, as potential interrupt handler latencies can become quite large. Even operating a serial port at maximum speed (115kbaud) can tax the resources of a system's latency periods, especially when such activity is talking place over the ISA bus (as is the case both with the serial ports and with the A/D FIFO). An interrupt rate of above 10 KHz can be difficult to sustain in Windows without the possibility of missing samples.

The A/D circuit uses the default settings of I/O address range 240h – 25Fh (base address 240) and IRQ 5. The IRQ setting can be changed if needed (via jumper block J4).



10.1 Data Acquisition Circuitry I/O Map

10.1.1 BASE ADDRESS

The data acquisition circuitry on Hercules-EBX occupies a block of 32 bytes in I/O memory space. The default address range for this block is 240h – 24Fh (base address 240). A functional list of registers is provided below, and detailed bit definitions are provided on the next page and in the following chapter.

The Address range is a 32-byte block in ISA I/O Space. Within these 32-bytes, the registers are paged to provide full access to additional registers for additional functions: 4 pages (0-3) are available. This page configuration is handled via the first register of the address space (located at the base address). Byte 0 is always present – it is mirrored across all 4 pages so that the page register is always available.

NOTE: all data is accurate as of "FPGA Design Specification Revision 1.79".

The Register lists for the three pages are as follows:

Page 0

Base +	Write Function	Read Function
0	Reset + page register	A/D LSB
1	Analog configuration register	A/D MSB
2	A/D low channel	A/D low channel readback
3	A/D high channel	A/D high channel readback
4	A/D range register	A/D range + status readback
5	D/A channel	-
6	D/A LSB	-
7	D/A MSB	-
8	FIFO threshold LSB	FIFO threshold LSB readback
9	FIFO threshold MSB	FIFO threshold MSB readback
10	-	FIFO depth LSB
11	-	FIFO depth MSB
12	Configuration register	Configuration register readback
13	Operation control register	Operation control register readback
14	-	Operation status register
15	Command register	Hardware config + A/D channel readback
16	DIO port A	DIO port A
17	DIO port B	DIO port B
18	DIO port C	DIO port C
19	DIO port D	DIO port D
20	DIO port E	DIO port E
21	-	-
22	DIO config / bit set	DIO config readback
23	-	-
24	Ctr/timer LSB	Ctr/timer LSB
25	Ctr/timer CSB	Ctr/timer CSB
26	Ctr/timer MSB	Ctr/timer MSB
27	Ctr command register	-
28	Watchdog timer A LSB	Watchdog timer A LSB
29	Watchdog timer A MSB	Watchdog timer A MSB
30	Watchdog timer B data	Watchdog timer B data
31	Watchdog configuration register	Watchdog config. register readback

Page 1

Base +	Write Function	Read Function
24	PWM data register LSB	PWM data register LSB
25	PWM data register CSB	PWM data register CSB
26	PWM data register MSB	PWM data register MSB
27	PWM configuration register	-
28	(Autocal) EEPROM / TrimDAC Data	(Autocal) EEPROM / TrimDAC Data
29	(Autocal) EEPROM / TrimDAC Address)	(Autocal) EEPROM / TrimDAC Address
30	(Autocal) Calibration Control register	(Autocal) Calibration Status register
31	(Autocal) EEPROM Access Key Register	FPGA Revision Code

Page 2

Base +	Write Function	Read Function
24	D/A waveform (future)	Feature ID register – A/D
25	D/A waveform (future)	Feature ID register – D/A
26	D/A waveform (future)	Feature ID register – DIO
27	D/A waveform (future)	Feature ID register – Ctr/timers
28	D/A waveform (future)	Device ID register
29	D/A waveform (future)	Device ID register
30	-	-
31	-	-

When pages 1 or 2 are enabled, the page 0 registers at addresses 0-23 are still accessible.

Page 3

Page 3 is a 27-byte page occupying locations 1-27 of the chip. This page contains a copyright notice in ASCII format.

In page 3, the RESET command and page register at base + 0 are still accessible, so the chip may be reset or the page may be changed.

REGISTER MAP BIT ASSIGNMENTS

PAGE 0 WRITE

Blank bits are unused and have no effect.

Offset	7	6	5	4	3	2	1	0
0	HOLDOFF	RESET					PAGE1	PAGE0
1						DABU	SEDIFF	ADBU
2				L4	L3	L2	L1	L0
3				H4	H3	H2	H1	H0
4	LDAD						G1	G0
5	SU						DACH1	DACH0
6	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
7					DA11	DA10	DA9	DA8
8	FT7	FT6	FT5	FT4	FT3	FT2	FT1	FT0
9					FT11	FT10	FT9	FT8
10								
11								
12	LED	SINGLE	DIOCTR1	DIOCTR0	SCINT	CLKSRC1	CLKFRQ1	CLKFRQ0
13		TINTE	DINTE	AINTE	FIFOEN	SCANEN	CLKSEL	CLKEN
14								
15			FIFORST	DARST	CLRT	CLRD	CLRA	ADSTART
16	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0
17	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0
18	DIOC7	DIOC6	DIOC5	DIOC4	DIOC3	DIOC2	DIOC1	DIOC0
19	DIOD7	DIOD6	DIOD5	DIOD4	DIOD3	DIOD2	DIOD1	DIOD0
20	DIOE7	DIOE6	DIOE5	DIOE4	DIOE3	DIOE2	DIOE1	DIOE0
21								
22	MODE	P2	P1	PO/DIRE	B2/DIRD	B1/DIRC	B0/DIRB	D/DIRA
23								
24	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0
25	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8
26	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16
27	CTR	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR
28	WDA7	WDA6	WDA5	WDA4	WDA3	WDA2	WDA1	WDA0
29	WDA15	WDA14	WDA13	WDA12	WDA11	WDA10	WDA9	WDA8
30	WDB7	WDB6	WDB5	WDB4	WDB3	WDB2	WDB1	WDB0
31	WDTRIG		WDEN	WDSMI	WDRST	WDT-1	WDEDGE	WDIEN

PAGE 0 READ

Blank bits are unused and read back as 0.

Offset	7	6	5	4	3	2	1	0
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2				L4	L3	L2	L1	L0
3				H4	H3	H2	H1	H0
4	ADBUSY	WAIT	DABUSY	DABU	SEDIFF	ADBU	G1	G0
5								
6								
7								
8	FT7	FT6	FT5	FT4	FT3	FT2	FT1	FT0
9					FT11	FT10	FT9	FT8
10	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
11				FD12	FD11	FD10	FD9	FD8
12	LED	SINGLE	DIOCTR1	DIOCTR0	SCINT	CLKSRC1	CLKFRQ1	CLKFRQ0
13		TINTE	DINTE	AINTE	FIFOEN	SCANEN	CLKSEL	CLKEN
14		TINT	DINT	AINT	OVF	FF	TF	EF
15	CFG1	CFG0		ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
16	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0
17	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0
18	DIOC7	DIOC6	DIOC5	DIOC4	DIOC3	DIOC2	DIOC1	DIOC0
19	DIOD7	DIOD6	DIOD5	DIOD4	DIOD3	DIOD2	DIOD1	DIOD0
20	DIOE7	DIOE6	DIOE5	DIOE4	DIOE3	DIOE2	DIOE1	DIOE0
21								
22				DIRE	DIRD	DIRC	DIRB	DIRA
23								
24	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0
25	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8
26	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16
27								
28	WDA7	WDA6	WDA5	WDA4	WDA3	WDA2	WDA1	WDA0
29	WDA15	WDA14	WDA13	WDA12	WDA11	WDA10	WDA9	WDA8
30	WDB7	WDB6	WDB5	WDB4	WDB3	WDB2	WDB1	WDB0

PAGE 1 WRITE

Blank bits are unused and have no effect.

Note that offsets 28, 29, and 31 refer to EEPROM Data, Address, and unlock command registers for Autocalibration

Offset	7	6	5	4	3	2	1	0
0	HOLDOFF	RESET					PAGE1	PAGE0
24								
25								
26								
27								
28	D7	D6	D5	D4	D3	D2	D1	D0
29		A6	A5	A4	A3	A2	A1	A0
30	EE_EN	EE_RW	RUNCAL	CMUXEN	TDACEN			

PAGE 1 READ

Blank bits are unused and read back as 0.

Note that offset 31 is the FPGA revision code (0x40 for this product).

Offset	7	6	5	4	3	2	1	0
0								
24	PWMD7	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMD0
25	PWMD15	PWMD14	PWMD13	PWMD12	PWMD11	PWMD10	PWMD9	PWMD8
26	PWMD23	PWMD22	PWMD21	PWMD20	PWMD19	PWMD18	PWMD17	PWMD16
27								
28	D7	D6	D5	D4	D3	D2	D1	D0
29		A6	A5	A4	A3	A2	A1	A0
30	0	TDBUSY	EEBUSY	CMUXEN	0	0	0	0

PAGE 2 WRITE

Blank bits are unused and have no effect.

Write registers 24-31 in this page are reserved for a future D/A waveform generator circuit.

Offset	7	6	5	4	3	2	1	0
0	HOLDOFF	RESET					PAGE1	PAGE0
24								
25								
26								
27								
28								
29								
30								

PAGE 2 READ

Blank bits are unused and read back as 0.

Offset	7	6	5	4	3	2	1	0
0								
24	ADQ7	ADQ6	ADQ5	ADQ4	ADQ3	ADQ2	ADQ1	ADQ0
25	FDID2	FDID1	FDID0	DAQ4	DAQ3	DAQ2	DAQ1	DAQ0
26	DIOQ7	DIOQ6	DIOQ5	DIOQ4	DIOQ3	DIOQ2	DIOQ1	DIOQ0
27	PWMQ3	PWMQ2	PWMQ1	PQMQ0	CTRQ3	CTRQ2	CTRQ1	CTRQ0
28	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
29	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
30								

10.1.2 PAGE 0 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

HOLDOFF When this bit is 1 the chip ignores any data written to this register. This bit is provided to enable shadowing this register with another device at the same address.

RESET Reset the entire data acquisition circuit. After a reset, the following conditions are true:

Digital I/O ports set to input mode and all output registers cleared to 0

A/D channel registers and range settings are cleared to 0 – **Except for Analog Configuration Register (Base + 1) which is set to 0x04**

D/A channels cleared to mid-scale or zero-scale depending on the board jumper setting

Counter/timers are disabled and counter registers cleared to 0

Watchdog timer is disabled and timer registers are cleared to 0

FIFO is reset, causing all contents to be lost, and threshold is set to 1024 samples

The internal channel / gain table is reset to all 0

PAGE1-0 Page no.:

0 Main features page

1 Extended features page

2 ID page

3 Copyright notice page

Base + 0 Read A/D LSB Register

Bit No.	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD7-0 A/D LSB data

The A/D data must be read LSB first, followed by MSB.

Base + 1 Write Analog Configuration Register

Bit No.	7	6	5	4	3	2	1	0
Name						DABU	SEDIFF	ADBU

The analog configuration register is typically written to once at the start of an application and then remains unchanged.

DABU 0 = bipolar, 1 = unipolar D/A output range **(Default on reset is unipolar mode)**

SEDIFF 0 = single-ended, 1 = differential A/D mode

ADBU 0 = bipolar, 1 = unipolar A/D input range

Note that these signal settings can be read back from Base + 4.

Base + 1 Read A/D MSB Register

Bit No.	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD15-8 A/D MSB data

The A/D data must be read LSB first, followed by MSB.

Base + 2 Read/Write A/D Low Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name				L4	L3	L2	L1	L0

L4-0 A/D low channel number

Base + 3 Read/write A/D High Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name				H4	H3	H2	H1	H0

AD15-8 A/D MSB data

Base + 4 Write A/D Input Range Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	LDAD						G1	G0

LDAD The FPGA contains a global input range setting as well as a 32x4 table for all 32 input channels that can be used for individual input ranges for each channel. The chip will use either the global input range setting or the individual range table based on the setting of the SINGLE bit in Base + 12.

If this bit is 1, the remaining bits are stored as the individual input range for the A/D channel currently set by L4-L0 in Base + 2. If this bit is 0, the remaining bits are the global setting for all input channels.

G1-0 Gain setting: 0 = gain of 1, 1 = gain of 2, 2 = gain of 4, 3 = gain of 8.

The gain is the ratio between the input voltage and the voltage seen by the A/D converter. The A/D always works with a maximum input voltage of 10V. A gain of 2 means the maximum input voltage at the connector pin is 5V.

Base + 4 Read A/D Range/Status Readback Register

Bit No.	7	6	5	4	3	2	1	0
Name	ADBUSY	WAIT	DABUSY	DABU	SEDIFF	ADBU	G1	G0

ADBUSY 1 = A/D is performing an A/D conversion; 0 = A/D is idle and data may be read out

WAIT 1 = A/D circuit is settling on a new channel or gain setting; program must not initiate an A/D conversion when WAIT = 1

0 = A/D circuit is ready to perform an A/D conversion

DABUSY 1 = D/A circuit is transferring data to the D/A chip after writing data to the board

0 = D/A circuit is idle / D/A output is stable

DABU 0 = bipolar, 1 = unipolar D/A output range

SEDIFF 0 = single-ended, 1 = differential A/D mode

ADBU 0 = bipolar, 1 = unipolar A/D input range

G1-0 Readback of global A/D gain setting; individual A/D gain settings may not be read back

Base + 5 Write D/A Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	SU						DACH1	DACH0

SU Simultaneous Update

0 = Transparent (written directly to the DAC's) / Simultaneous Write

1 = Latch and hold data (DAC output not updated until "0" is written later)

DACH1-0 D/A channel number

Writing to this register updates the selected D/A channel with the data currently stored in Base + 6 and Base + 7. The high-order bit determines whether the data is transferred directly out to the DAC's (transparent mode) or is latched and held for a later simultaneous update.

Base + 6 Write D/A LSB Register

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA7-0 D/A LSB data

Base + 7 Write D/A MSB Register

Bit No.	7	6	5	4	3	2	1	0
Name	DA15	DA14	DA12	DA12	DA11	DA10	DA9	DA8

DA15-8 D/A MSB data

Base + 8 Read/Write FIFO Threshold Register LSB

Bit No.	7	6	5	4	3	2	1	0
Name	FT7	FT6	FT5	FT4	FT3	FT2	FT1	FT0

FT7-0 FIFO threshold value LSB

Base + 9 Read/Write FIFO Threshold Register MSB

Bit No.	7	6	5	4	3	2	1	0
Name						FT10	FT9	FT8

FT11-8 FIFO threshold value MSB

When the FIFO depth is greater than or equal to the FIFO threshold, TF (threshold flag) = 1 and an A/D interrupt request will be generated if FIFOEN = 1 and ADINTE = 1.

The FIFO size is 2048 samples. The threshold value may be anywhere from 1 to 2047 samples. In most cases the threshold does not need to be larger than 1/2 the FIFO size, or 1024 samples.

On power-up or system reset, the FIFO threshold is reset to 1024 samples.

Base + 10 Read FIFO Depth Register LSB

Bit No.	7	6	5	4	3	2	1	0
Name	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

FD7-0 Current FIFO depth LSB

Base + 11 Read FIFO Depth Register MSB

Bit No.	7	6	5	4	3	2	1	0
Name				FD12	FD11	FD10	FD9	FD8

FD12-8 Current FIFO depth MSB

The FIFO depth register indicates the current depth, or no. of bytes, in the FIFO. The depth is reset to 0 when a FIFORST command occurs. It increments by 1 each time a byte from the A/D converter is inserted into the FIFO and decrements by 1 each time a byte is read out. FD therefore increments / decrements by 2 for a full A/D sample write or read operation. Note that if a 16-bit read operation occurs, FD decrements by 2 after the operation.

Base + 12 Read/Write Configuration Register

Bit No.	7	6	5	4	3	2	1	0
Name	LED	SINGLE	DIOCTR1	DIOCTR0	SCINT	CLKSRC1	CLKFRQ1	CLKFRQ0

LED Active high – simple status bit used to drive external LED (active high). Default should be high upon power-up.

SINGLE Indicates whether to use the global A/D input range or the individual input range table for A/D conversions.

0 = use global setting for all channels, 1 = use the programmed settings for each channel.

DIOCTR1 0 = digital I/O lines DIOE7-4 appear on DIOE7-4 pins of I/O connectors
1 = counter signals appear on DIOE7-4 pins of I/O connectors

DIOCTR0 0 = digital I/O lines DIOE3-0 appear on DIOE3-0 pins of I/O connectors
1 = PWM signals appear on DIOE3-0 pins of I/O connectors

SCINT A/D scan interval selection; 0 = 4µS, 1 = 9µS

CLKSRC1 Clock source for counter 1: 0 = internal (see CLKFRQ1 below), 1 = external

CLKFRQ1 Internal clock frequency for counter 1: 0 = 10MHz, 1 = 100 KHz

CLKFRQ0: Internal clock frequency for counter 0: 0 = 10MHz, 1 = 100 KHz

Base + 13 Read/Write Operation Control Register

Bit No.	7	6	5	4	3	2	1	0
Name		TINTE	DINTE	AINTE	FIFOEN	SCANEN	CLKSEL	CLKEN

TINTE Timer interrupt enable: 0 = disabled, 1 = enabled

DINTE Digital I/O interrupt enable: 0 = disabled, 1 = enabled

AINTE A/D interrupt enable: 0 = disabled, 1 = enabled

Only one of the above three interrupts may be enabled at a time.

FIFOEN FIFO enable: 0 = disabled, 1 = enabled

When the FIFOEN = 1 and AINTE = 1, A/D interrupts will occur when the FIFO reaches its programmed threshold set with FT11-0. When FIFOEN = 0 and AINTE = 1, A/D interrupts will occur as follows: If SCANEN = 1, the interrupt will occur at the end of the scan, and the FIFO will contain all the samples of the scan. If SCANEN = 0, the interrupt will occur after each single A/D conversion.

SCANEN A/D Scan enable: 0 = disabled, 1 = enabled

When SCANEN = 1, the A/D circuit will perform a complete scan of all channels between the low and high channels, inclusive, upon each trigger.

CLKEN A/D hardware clock enable: 0 = disabled, 1 = enabled

When CLKEN = 1, the A/D circuit is triggered by the hardware clock selected with CLKSEL below, and software A/D trigger is disabled.

CLKSEL A/D hardware clock select, only applies when CLKEN = 1:

0 = rising edge of counter/timer 0

1 = falling edge on external trigger from I/O connector

Base + 14 Read Operation Status Register

Bit No.	7	6	5	4	3	2	1	0
Name		TINT	DINT	AINT	OVF	FF	TF	EF

TINT Timer interrupt status: 1 = interrupt pending, 0 = no interrupt pending

DINT Digital I/O interrupt status: 1 = interrupt pending, 0 = no interrupt pending

AINT A/D interrupt status: 1 = interrupt pending, 0 = no interrupt pending

OVF FIFO overflow flag: 0 = no overflow, 1 = overflow

Overflow occurs when the FIFO is full and an A/D conversion occurs. If OVF is set, it will stay set until the FIFO is reset with a FIFORST command.

FF FIFO full flag: 0 = FIFO is not full, 1 = FIFO is full

TF FIFO threshold flag: 0 = FIFO depth is below the programmed threshold, 1 = FIFO depth is at or above the programmed threshold

EF FIFO empty flag: 0 = not empty, 1 = empty

Base + 15 Write Command Register

Bit No.	7	6	5	4	3	2	1	0
Name			FIFORST	DARST	CLRT	CLRD	CLRA	ADSTART

Each bit in this register represents a command. Writing a 1 to any bit executes the command specified by that bit. Only one bit may be written to at a time.

FIFORST Reset the FIFO; after this command, OVF, FF, and TF = 0, and EF = 1

DARST Reset the D/A; all D/A channels will reset to zero-scale

CLRT Clear timer interrupt request

CLRD Clear digital I/O interrupt request

CLRA Clear A/D interrupt request

ADSTART Start an A/D conversion; after this command, ADBUSY = 1 until the A/D conversion is finished

Base + 15 Read Hardware Configuration and A/D Channel Readback

Bit No.	7	6	5	4	3	2	1	0
Name	CFG1	CFG0		ADCH4	ADCH3	ADCH2	ADCH1	ADCH0

CFG1-0 These bits report the logic level of two input pins on the logic chip that can be used to indicate the board's hardware configuration. Currently defaults to "11".

ADCH4-0 Current A/D channel; this is the channel that will be sampled on the next A/D conversion.

Base + 16 Read/Write Digital I/O Port A

Bit No.	7	6	5	4	3	2	1	0
Name	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0

Base + 17 Read/Write Digital I/O Port B

Bit No.	7	6	5	4	3	2	1	0
Name	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0

Base + 18 Read/Write Digital I/O Port C

Bit No.	7	6	5	4	3	2	1	0
Name	DIOC7	DIOC6	DIOC5	DIOC4	DIOC3	DIOC2	DIOC1	DIOC0

Base + 19 Read/Write Digital I/O Port D

Bit No.	7	6	5	4	3	2	1	0
Name	DIOD7	DIOD6	DIOD5	DIOD4	DIOD3	DIOD2	DIOD1	DIOD0

Base + 20 Read/Write Digital I/O Port E

Bit No.	7	6	5	4	3	2	1	0
Name	DIOE7	DIOE6	DIOE5	DIOE4	DIOE3	DIOE2	DIOE1	DIOE0

Port E shares device pins with 4 counter/timer signals and 4 PWM outputs. The function of these two groups of 4 pins is controlled with register bits DIOCTR1 and DIOCTR0:

DIOCTR1 0 = digital I/O lines DIOE7-4 appear on DIOE7-4 pins of I/O connectors
1 = counter signals appear on DIOE7-4 pins of I/O connectors

DIOCTR0 0 = digital I/O lines DIOE3-0 appear on DIOE3-0 pins of I/O connectors
1 = PWM signals appear on DIOE3-0 pins of I/O connectors

(See Base + 12 Configuration Register for details)

Base + 22 Write Digital I/O Configuration / Bit Programming Register

Bit No.	7	6	5	4	3	2	1	0
Name	MODE	P2	P1	PO/DIRE	B2/DIRD	B1/DIRC	B0/DIRB	D/DIRA

MODE Indicates port direction or bit programming mode: 0 = port direction, 1 = bit programming

When MODE = 1, this register provides a quick way to program individual digital I/O bits:

P2-0 Port no.: A = 0, B = 1, C = 2, D = 3, E = 4

B2-0 Bit no., 0-7

D Bit value, 0 or 1

When MODE = 0, this register is used to configure the direction of the digital I/O ports:

DIRE-A Direction for ports A – E: 0 = input, 1 = output

On power-up or system reset, all ports are set to input mode and the contents of the output registers are set to 0.

Base + 24 Read/Write Counter/Timer Data Register Byte 1

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0

CTRD7-0 LSB for counter/timers 0 and 1

Base + 25 Read/Write Counter/Timer Data Register Byte 2

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8

CTRD15-8 CSB (middle byte) for counter/timer 0, MSB for counter/timer 1

Base + 26 Read/Write Counter/Timer Data Register Byte 3

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16

CTRD23-16 MSB for counter/timer 0

Counter/timer 0 is 24 bits wide and uses all three bytes. Counter/timer 1 is 16 bits wide and uses only bytes 1 and 2. The bytes may be written and read in any order.

Base + 27 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTR	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

CTR Counter no., 0 or 1

LATCH Latch selected counter's current data into bytes 1-3 or 1-2 as appropriate

GTDIS Disable gating on selected counter

GTEN Enable gating on selected counter

CTDIS Disable counting on selected counter

CTEN Enable counting on selected counter

LOAD Load selected counter with data in bytes 1-3 or 1-2 as appropriate

CLR Clear selected counter to 0

Base + 28 Read/Write Watchdog Timer A LSB Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDA7	WDA6	WDA5	WDA4	WDA3	WDA2	WDA1	WDA0

WDA7-0 LSB of timer A divisor; loading occurs for both bytes when the MSB is written

Base + 29 Read/Write Watchdog Timer A MSB Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDA15	WDA14	WDA13	WDA12	WDA311	WDA10	WD9	WD80

WDA15-8 MSB of timer A divisor; loading occurs for both bytes when the MSB is written

Base + 30 Read/Write Watchdog Timer B Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDB7	WDB6	WDB5	WDB4	WDB3	WDB2	WDB1	WDB0

WDB7-0 Watchdog timer B data register; loading occurs immediately upon writing to this register.

Base + 31 Read/Write Watchdog Timer Configuration Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDTRIG		WDEN	WDSMI	WDRST	WDT-1	WDEDGE	WDIEN

WDTRIG If this bit is 1, the remaining bits of this register are ignored and instead the watchdog timer A is retriggered, i.e. reloaded with its initial value. If this bit is 0, the remaining bits in this register are used to configure the watchdog timer circuit.

WDEN Enable watchdog timer circuit: 0 = disabled, 1 = enabled

WDSMI Enable SMI interrupt upon watchdog timer timeout

WDRST Enable system reset upon watchdog timer timeout (setting this clears WDSMI)

WDT-1 Enable output pulse from timer A 1 clock early on WDO pin of I/O connectors. This allows WDO to be connected to WDI to prevent watchdog timer timeout as long as the timer is running.

WDEDGE Select active edge for hardware (external) retrigger: 0 = rising edge, 1 = falling edge

WDIEN Enable external input hardware watchdog trigger instead of on-board software trigger:

0 = internal trigger only, 1 = external trigger plus internal trigger are enabled

10.1.3 PAGE 1 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

See page 0 for the definition of this register.

Base + 24 Write PWM Data Register LSB

Bit No.	7	6	5	4	3	2	1	0
Name	PWMD7	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMD0

PWMD7-0 PWM data bits 7-0

Base + 25 Write PWM Data Register CSB

Bit No.	7	6	5	4	3	2	1	0
Name	PWMD15	PWMD14	PWMD13	PWMD12	PWMD11	PWMD10	PWMD9	PWMD8

PWMD15-8 PWM data bits 15-8

Base + 26 Write PWM Data Register MSB

Bit No.	7	6	5	4	3	2	1	0
Name	PWMD23	PWMD22	PWMD21	PWMD20	PWMD19	PWMD18	PWMD17	PWMD16

PWMD23-16 PWM data bits 23-16

Base + 27 Write PWM Command Register

This register serves two purposes based on the value of bit 7, PCMD. Bit 7 = 0 indicates a PWM command, and bit 7 = 1 indicates a configuration command.

Bit No.	7	6	5	4	3	2	1	0
Name	0	0	PWM1	PWM0	0	0	0	CTR

0 Indicates a PWM command

0 Reserved for future use

PWM1-0 Indicates which PWM circuit is being accessed

000 Indicates a load counter command; this is the only command currently defined

CTR Indicates which counter to act on: 0 = rate counter, 1 = duty cycle counter

The above may also be thought of as two commands: 00..000 = load ctr 0, and 00..001 = load ctr 1.

Bit No.	7	6	5	4	3	2	1	0
Name	1	0	PWM1	PWM0	CLK	POL	OUTEN	ENAB

1 Indicates a PWM configuration byte

0 Reserved for future use

PWM1-0 Indicates which of the 4 PWM circuits is being accessed

CLK Selects internal clock source for both PWM counters: 0 = 10MHz, 1 = 100 KHz

POL Selects polarity of output pulse (active level): 0 = active low level, 1 = active high level

OUTEN Output enable: 0 = disabled (output held at inactive level based on setting of POL bit), 1 = enabled

ENAB PWM enable: 0 = disabled; 1 = running

Base + 28 Read/Write EEPROM / TrimDAC Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-0 Calibration data to be read or written to the EEPROM and/or TrimDAC.

During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.

During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after EEBUSY = 0.

The EEPROM data can be both read and written. The TrimDAC data can only be written; it cannot be read back.

Base + 29 Read/Write EEPROM / TrimDAC Address Register

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

A7-A0 EEPROM / TrimDAC address. The EEPROM recognizes address 0 – 255 using address bits A7 – A0. The TrimDAC recognizes addresses 0 – 7 using bits A2 – A0. In each case remaining address bits will be ignored.

NOTE: Current implementations of FPGA/Data Acquisition storage only take advantage of the lower 128 bytes of EEPROM data at the most. The remaining 128 bytes (addresses 128-255) are available for general use.

Base + 30 Write Calibration Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	EE_EN	EE_RW	RUNCAL	CMUXEN	TDACEN			

This register is used to initiate various commands related to autocalibration.

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit. However if TDACEN is set simultaneously, EE_EN is ignored.

EE_RW Selects read or write operation for the EEPROM: 0 = Write, 1 = Read.

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM registers 0-7 into the 8 TrimDACs. This is equivalent to a “reload” operation. During the reload operation, TDBUSY = 1.

CMUXEN Calibration multiplexer enable. The CMUXEN bit is used to enable calibration mode. After calibration is complete, CMUXEN is reset and the desired configuration is restored. The cal mux is used to read precision on-board reference voltages that are used in the autocalibration process. It also can be used to read back the value of analog output 0.

1 = enable cal mux and disable user analog input channels / muxes

0 = disable cal mux, enable user inputs

TDACEN TrimDAC Enable. Writing 1 to this bit will initiate a transfer to the TrimDAC. This bit overrides the setting of EE_EN, so that if both bits are set simultaneously, EE_EN will be ignored.

Base + 30 Read Calibration Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	0	TDBUSY	EEBUSY	CMUXEN	0	0	0	0

TDBUSY TrimDAC busy indicator

0 User may access TrimDAC

1 TrimDAC is being accessed or reload operation is in progress

EEBUSY EEPROM busy indicator

0 User may access EEPROM

1 EEPROM is being accessed

When either signal is 1, do not access the data and address registers at base + 12 and base + 13.

Base + 31 Write EEPROM Access Key Register

The user must write the value 0xA5 (binary 10100101) to this register each time after setting the PAGE bit in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents.

Base + 31 Read FPGA Revision Code

This register may be read back to indicate the revision number of the FPGA design. The revision code for this design is 0x40.

10.1.4 PAGE 2 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

See page 0 for the definition of this register.

Base + 24 Read A/D Feature ID Register

Bit No.	7	6	5	4	3	2	1	0
Name	ADQ7	ADQ6	ADQ5	ADQ4	ADQ3	ADQ2	ADQ1	ADQ0

ADQ7-0 Indicates the number of A/D channels available on the board

Base + 25 Read D/A Feature ID & FIFO Depth ID Register

Bit No.	7	6	5	4	3	2	1	0
Name	FDID2	FDID1	FDID0	DAQ4	DAQ3	DAQ2	DAQ1	DAQ0

FDID2-0 Indicates the maximum sample depth supported by the FPGA FIFO. Currently, only a value of “001” is defined, which describes a FIFO depth of 2048 samples.

DAQ4-0 Indicates the number of D/A channels available on the board

Base + 26 Read Digital I/O Feature ID Register

Bit No.	7	6	5	4	3	2	1	0
Name	DIOQ7	DIOQ6	DIOQ5	DIOQ4	DIOQ3	DIOQ2	DIOQ1	DIOQ0

DIOQ7-0 Indicates the number of DIO pins available on the board

Base + 27 Read PWM and Ctr/Timer Feature ID Register

This register serves two purposes based on the value of bit 7. Bit 7 = 0 indicates a load counter command, and bit 7 = 1 indicates a configure command.

Bit No.	7	6	5	4	3	2	1	0
Name	PWMQ3	PWMQ2	PWMQ1	PQMQ0	CTRQ3	CTRQ2	CTRQ1	CTRQ0

PWMQ3-0 Indicates the number of PWM channels available on he board

CTRQ3-0 Indicates the number of counter/timers available on the board

Base + 28 Read Chip ID LSB

Bit No.	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Base + 29 Read CHIP ID MSB

Bit No.	7	6	5	4	3	2	1	0
Name	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

ID15-0 Indicates the unique chip ID according to a format TBD. Each revision of the chip, whether prototype or production, standard or custom, contains a unique 16-bit ID to enable software to distinguish between different versions.

ID15 = 0 indicates a prototype / unreleased version, and ID15 = 1 indicates a released design.

The current revision code (as per this document) should be 0x8000 or higher, as per the prototype / production criteria listed above.

10.1.5 PAGE 3 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

See page 0 for the definition of this register.

Base + 1-31 Read Copyright Notice

The remaining bytes 1-31 in page 3 are read-only and contain a copyright notice in 8-bit ASCII format.

10.2 Data Acquisition Circuit Configuration

There are three primary configuration options for the Data Acquisition circuitry on the Hercules-EBX board:

- (A/D) : single-ended versus differential
- (A/D) : unipolar or bipolar
- (D/A) : unipolar or bipolar

These settings are all configured in software – no jumper configurations are required for these options. All of these settings are configured in the register located in PAGE 0; offset Base +1 (Analog Configuration register):

- Bit 0 = ADBU 0 = bipolar, 1 = unipolar A/D input range
- Bit 1 = SEDIFF 0 = single-ended, 1 = differential A/D mode
- Bit 2 = DABU 0 = bipolar, 1 = unipolar D/A output range (Default on reset is unipolar mode)

Single-ended / Differential Inputs

Hercules-EBX can accept both single-ended and differential inputs. A **single-ended** input uses 2 wires, input and ground. The measured input voltage is the difference between these two wires. A **differential** input uses 3 wires: input +, input -, and ground. The measured input voltage is the difference between the + and - inputs.

Differential inputs are frequently used when the grounds of the input device and the measurement device (Hercules-EBX) are at different voltages, or when a low-level signal is being measured that has its own ground wire. A differential input also has higher noise immunity than a single-ended input, since most noise affects both + and – input wires equally, so the noise will be canceled out in the measurement. The disadvantage of differential inputs is that only half as many are available, since two input pins are required to produce a single differential input. Hercules-EBX can be configured for either 32 single-ended inputs or 16 differential inputs.

If you have a combination of single-ended and differential input signals, select differential mode. Then to measure the single-ended signals, connect the signal to the + input and connect analog ground to the - input.

Note that the maximum measureable rail voltage is +/- 10V for differential inputs : any voltage outside of this range will measure as at the maximum rail (so if VIN0+ = +15V and VIN0-=+10V the differential voltage will measure as 0V since both voltages are outside of the maximum measureable range).

WARNING: The maximum range of voltages that can be applied to an analog input on Hercules-EBX without damage is ±35V. If you connect the analog inputs on Hercules-EBX to a circuit whose ground potential plus maximum signal voltage exceeds ±35V, the analog input circuit may be damaged. Check the ground difference between the input source and Hercules-EBX before connecting analog input signals.

Unipolar / Bipolar Inputs

The analog inputs can be configured for unipolar (positive input voltages only) or bipolar (both negative and positive input voltages).

Analog Output Configuration

The 4 analog outputs can also be configured for unipolar (positive voltages only) or bipolar (both negative and positive output voltages). In unipolar mode, the outputs range between 0-10V. In bipolar mode, the outputs range between ±10V.

When the board powers up or is reset, the analog outputs are also reset. The D/A powers up in unipolar mode with zero-scale output (0V default).

10.3 Analog Input Ranges and Resolution

10.3.1 OVERVIEW

Hercules-EBX uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However the A/D converter uses twos complement notation, so the A/D value is interpreted as a signed integer ranging from –32768 to +32767.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and so this change is referred to as 1 LSB, or 1 Least Significant Bit.

The analog inputs on Hercules-EBX have three configuration options:

- Single-ended or differential mode
- Unipolar or bipolar mode
- Input range (gain)

The single-ended / differential configuration, unipolar / bipolar configuration, and the input range selection are all handled in software.

10.3.2 INPUT RANGE SELECTION

Hercules-EBX can be configured to measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. This configuration is done via the Analog Configuration Register (Page 0:Base+1) and applies to all inputs. In addition you can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software, so it can be changed on a channel-by-channel basis. In general you should select the highest gain (smallest input range) that will allow the A/D converter to read the full range of voltages over which your input signals will vary. If you pick too high a gain, then the A/D converter will clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

10.3.3 INPUT RANGE TABLE

The table below indicates the analog input range for each possible configuration. The polarity is set in the Analog Configuration Register (Page 0:Base+1), and the gain is set with the G1 and G0 bits in the Input Range Control Register (Page 0:Base+4). The Gain value in the table is provided for clarity. Note that the single-ended vs. differential setting has no impact on the input range or the resolution.

Polarity	G1	G0	Input Range	Resolution (1 LSB)
Bipolar	0	0	±10V	305µV
Bipolar	0	1	±5V	153µV
Bipolar	1	0	±2.5V	76µV
Bipolar	1	1	±1.25V	38µV
Unipolar	0	0	0 – 10V	153µV
Unipolar	0	1	0 – 5V	76µV
Unipolar	1	0	0 – 2.5V	38µV
Unipolar	1	1	0 – 1.25V	19µV

Table 33: Data Acquisisition : Analog Input Range

10.4 Performing an A/D Conversion

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (not with the driver software).

There are seven steps involved in performing an A/D conversion:

1. **Select the input channel**
2. **Select the input range**
3. **Wait for analog input circuit to settle**
4. **Initiate an A/D conversion**
5. **Wait for the conversion to finish**
6. **Read the data from the board**
7. **Convert the numerical data to a meaningful value**

10.4.1 SELECT THE INPUT CHANNEL

To select the input channel to read, write a low-channel/high-channel pair to the "A/D Low Channel Register" (Page 0:Base+2) and "A/D High Channel Register" (Page 0:Base+3) pair (see page 63). For the Hercules-EBX, only 5 bits are supported for each setting: "0"-"31" for the 32 potential input source channels. When you write any value to these registers, the current A/D channel is set to the low channel.

For example:

To set the board to channel 4 only, write 0x04 to Base + 2 (low channel) and 0x04 to Base + 3 (high channel).

To set the board to read channels 0 through 15, write 0x00 to Base + 2 (low channel) and 0x0F to Base + 3 (high channel).

Þ **Note:** When you perform an A/D conversion, the current channel is automatically incremented to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write Hex 00 to base + 2 and Hex 02 to base +3. The first conversion is on channel 0, the second will be on channel 1, and the third will be on channel 2. Then the channel counter wraps around to the beginning again, so the fourth conversion will be on channel 0 again and so on.

If you are sampling the same channel repeatedly, then you set both high and low to the same value as in the first example above. Then on subsequent conversions you do not need to set the channel again.

10.4.2 SELECT THE INPUT RANGE

Select the input range from among the available ranges shown on page 79. If the range is the same as for the previous A/D conversion then it does not need to be set again. Write this value to the A/D Input Range Control Register at Base + 4 (see page 64).

For example:

For a global (affects all channels) ±5V range (gain of 2), write 0x01 to Base + 4.

10.4.3 WAIT FOR ANALOG INPUT CIRCUIT TO SETTLE

After writing to either the channel registers (Base + 2, Base +3) or the input range register (Base + 4), you must allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10µS timer to assist with the wait period. Monitor the WAIT bit at Base + 4 bit 6. When it is 1 the circuit is actively settling on the input signal. When it is 0 the board is ready to perform A/D conversions.

10.4.4 PERFORM AN A/D CONVERSION ON THE CURRENT CHANNEL

After the above steps are completed, start the A/D conversion by writing to Base + 15, bit 0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base +15,0x01);
```

10.4.5 WAIT FOR THE CONVERSION TO FINISH

The A/D converter chip takes up to either 4 or 9 microseconds to complete one A/D conversion, depending on the scan interval setting (Base + 12 : bit 3). Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, you will beat the A/D converter and get invalid data. Therefore the A/D converter provides a status signal, “ADBUSY,” to indicate whether it is busy or idle. This bit can be read back as bit 7 in the “A/D Range/Status Readback Register“ at Page 0 : Base+4. When the A/D converter is busy (performing an A/D conversion), this bit is 1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), this bit is 0 and the program may read the data. Here are examples:

```
while (inp(base+4) & 0x80);    // Wait for conversion to finish before proceeding
```

This method could hang your program if there is a hardware fault and the bit is stuck at 1. Better is to use a loop with a timeout:

```
int checkstatus()       // returns 0 if ok, -1 if error
    int i;
    for (i = 0; i < 10000; i++)
    {
        if !(inp(base+4) & 0x80) then return(0);          // conversion completed
    }
    return(-1);         // conversion didn't complete
```

10.4.6 READ THE DATA FROM THE BOARD

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and can be read back as either two 8-bit bytes or one 16-bit word. For 8-bit accesses, the LSB must be read from the board before the MSB, because the data is inserted into the board’s FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, since each time a byte is read from the FIFO, the FIFO’s internal pointer advances, and that byte is no longer available. Note that reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value with 8-bit accesses:

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

Alternatively, the value can be read as one 16-bit value (which is preferred – this would increase the overall system bandwidth while reading data from the FIFO):

```
Data = inpw(base); // Where the MSB and LSB are all read in one access
```

The final data is interpreted as a 16-bit signed integer ranging from –32768 to +32767. The “A/D LSB Register” and “A/D LSB Register” can be combined into one 16-bit read. These two registers fully support 16-bit I/O reads (in hardware), so the most efficient I/O method would be to read the two bytes as a single 16-bit word.

Þ **Note:** The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula as shown on the next page.

In scan mode, the behavior is the same except that when the program initiates a conversion, all channels in the programmed channel range will be sampled once, and the data will be stored in the FIFO. The FIFO depth register will increment by the scan size. When ADBUSY goes low, the program should read out the data for all channels.

10.4.7 CONVERT THE NUMERICAL DATA TO A MEANINGFUL VALUE

Once you have the A/D value, you need to convert it to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards you may need to convert the voltage to some other engineering units (for example, the voltage may come from a temperature sensor, and then you would need to convert the voltage to the corresponding temperature according to the temperature sensor's characteristics).

Since there are a large number of possible input devices, this secondary step is not included here; only conversion to input voltage is described. However you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas:

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input range

Example: Input range is ±5V and A/D value is 17761:
Input voltage = 17761 / 32768 * 5V = 2.710V

For a bipolar input range, 1 LSB = 1/32768 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a bipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for ±5V range
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
…	…	…
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
…	…	…
32767	V_{FS} - 1 LSB	4.9998V

Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D value + 32768) / 65536 * Full-scale input range

Example: Input range is 0-5V and A/D value is 17761:
Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a unipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for 0-5V range
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.000076V
…	…	…
-1	V_{FS} / 2 - 1 LSB	2.4999V
0	V_{FS} / 2	2.5000V
1	V_{FS} / 2 + 1 LSB	2.5001V
…	…	…
32767	V_{FS} - 1 LSB	4.9999V

10.5 A/D Scan, Interrupt, and FIFO Operation

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

At the end of an A/D conversion, the 16-bit A/D data is latched into the 8-bit FIFO in an interleaved fashion, first LSB, and then MSB. A/D Data is read out of the FIFO with 1 16-bit or 2 8-bit read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in the A/D Low Channel Register (Base + 2) and A/D High Channel Register (Base + 3). When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation (AINTE = 1), the FIFO will fill up with data until it reaches the threshold programmed in the FIFO threshold register, and then the interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

The FIFO Threshold Registers should be set to the desired depth before configuring the system to begin operation in interrupt mode. The maximum FIFO depth can be read from the FIFO Depth ID Register (Page 2: Base + 25): This register should always return a value of a value of "001" for the FIFO ID: means a maximum depth of 2048 samples.

To set the FIFO depth, the FIFO Threshold should be configured by writing the depth (in samples) to the "FIFO Threshold Register LSB" (Page 0: Base + 8) and "FIFO Threshold Register MSB" (Page 0: Base + 9). Note that this setting is in units of "samples", where one "sample" is 2 bytes. The current maximum setting would be 2047 (Base + 8 = Hex FF; Base + 9 = 0x07).

If the FIFO reaches its limit (as set in the two FIFO Threshold Registers located at Page 0: Base +8 and Base +9), then the next time an A/D conversion occurs the FIFO Threshold flag (Base + 14 : bit 3) would be set. At the same time, an interrupt would be generated (if FIFOEN = 1 and ADINTE = 1).

If the FIFO overflows, then the Overflow flag OVF will be set as the 2049th sample is taken. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the FIFORST bit in Base + 15, or a hardware reset must occur.

Note that the current FIFO state can be read at any time by checking the two FIFO Depth Registers: "FIFO Depth Register LSB" at Page 0: Base + 10 and "FIFO Depth Register MSB" at Page 0: Base + 11. These registers will return the number of samples currently in the FIFO. They are incremented with each A/D converter sample stored and are decremented with every FIFO sample read out (via the A/D LSB Register and A/D MSB register located at Base+0 and Base + 1, respectively).

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold could be set to 8, 16, 24, 32, 40, 48, etc. but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the next A/D conversion occurs. Remember that no data is available until the interrupt occurs, so if the rate is slow the delay to receive A/D data may be long. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS. Experimentation may be necessary to determine the optimum FIFO threshold for each application.

The table on the next page describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN. The given interrupt software behavior describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

10.6 Hercules-EBX A/D Operating Modes

The following control bits and values are referenced in the descriptions in the table below.

LOW	Page 0: Base + 2 (5-bit number, 0-31)
HIGH	Page 0: Base + 3 (5-bit number, 0-31)
WAIT	Page 0: Base + 4, bit 6
ADBUSY	Page 0: Base + 4, bit 7
FIFO threshold	Page 0: Base + 8 (LSB), Base + 9 (MSB)
CLKEN	Page 0: Base +13, bit 0
CLKSEL	Page 0: Base +13, bit 1
SCANEN	Page 0: Base + 13 bit 2
AINTE	Page 0: Base + 13 bit 4
ADSTS	signal from A/D Converter (called "BUSY" at A/D output)

There are 8 cases to consider for A/D conversions using FIFOEN, SCANEN, and AINTE.

In all cases, at the end of an AD conversion A/D data is latched into the FIFO. Data is read out of the FIFO with 2 read operations, nominally from Base+ 0 and Base + 1. However reading from either address will result in the same byte being read from the FIFO, so the program can actually perform 2 reads from the same address to get the A/D data. For all cases where AINTE = 1, CLKEN must also be set to 1.

AINTE	FIFOEN	SCANEN	Operation
0	0	0	Single A/D conversions are triggered by write to Base+15, bit 0. ADBUSY = ADSTS (from A/D) No interrupt occurs. The user program monitors ADBUSY and reads A/D data when it goes low.
0	0	1	A/D Scans are triggered by write to Base+15, bit 0. All channels between LOW and HIGH will be sampled. WAIT goes high at the first ADBUSY high pulse and stays high until the last ADBUSY pulse goes low. No interrupt occurs. The user program monitors WAIT and then reads the A/D data when it goes low.
0	1	0	Same operation as case 000 above. The FIFO is not used in this case.
0	1	1	Same operation as case 001 above. The FIFO is not used in this case.
1	0	0	Single A/D conversions are triggered by the source selected with CLKSEL. ADBUSY = ADSTS INT goes high after each conversion is done (when ADBUSY goes low). The interrupt routine reads one A/D sample each time it runs.
1	0	1	A/D Scans are triggered by the source selected with CLKSEL. WAIT goes high at the first ADBUSY high pulse and stays high until the last ADBUSY pulse goes low. INT goes high after the last ADBUSY pulse goes low (i.e. when WAIT goes low). The interrupt routine reads out one entire A/D scan each time it runs.
1	1	0	Single A/D conversions are triggered by the source selected with CLKSEL. ADBUSY = ADSTS A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads out a number of samples equal to the FIFO threshold each time it runs.
1	1	1	A/D scans are triggered by the source selected with CLKSEL. WAIT goes high at the first ADBUSY high pulse and stays high until the last ADBUSY pulse goes low. INT goes high after the last ADBUSY pulse goes low (i.e. when WAIT goes low) AND an integral no. of scans has occurred and the FIFO threshold is reached. The interrupt routine reads out a number of samples equal to the FIFO threshold each time it runs.

Table 34: A/D Operating Modes

10.7 Analog Output Ranges and Resolution

10.7.1 DESCRIPTION

Hercules-EBX uses a 4-channel 12-bit D/A converter (DAC) to provide 4 analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB (the theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve).

Þ **Note:** In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from the Hercules-EBX computer hardware to an analog signal terminating at an external source.

10.7.2 RESOLUTION

The *resolution* is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, and so this change is referred to as 1 LSB, or 1 least significant bit. The value of this LSB is calculated as follows:

1 LSB = Output voltage range / 4096

Example: Output range = 0-10V;

Output voltage range = 10V – 0V = 10V

1 LSB = 10V / 4096 = 2.44mV

Example: Output range = ±10V;

Output voltage range = 10V – (-10V) = 20V

1 LSB = 20V / 4096 = 4.88mV

10.7.3 OUTPUT RANGE SELECTION

The Analog Configuration Register located at Page 0: Base +1 is used to select the DAC output range. See page 63 for configuration data. The DACs can be configured for 0-10V or ±10V.

10.7.4 D/A CONVERSION FORMULAS AND TABLES

The formulas below explain how to convert between D/A codes and output voltages.

D/A Conversion Formulas for Unipolar Output Ranges

Output voltage = (D/A code / 4096) * Reference voltage

D/A code = (Output voltage / Reference voltage) * 4096

Example: Output range in unipolar mode = 0 – 10V
Full-scale range = 10V – 0V = 10V
Desired output voltage = 2.000V
D/A code = 2.000V / 10V * 4096 = 819.2 => 819

Note the output code is always an integer.

For the unipolar output range 0-10V, 1 LSB = 1/4096 * 10V = 2.44mV.

Here is an illustration of the relationship between D/A code and output voltage for a unipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for 0 – 10V range
0	0V	0.0000V
1	1 LSB (V_{REF} / 4096)	0.0024V
…	…	…
2047	V_{REF} / 2 - 1 LSB	4.9976V
2048	V_{REF} / 2	5.0000V
2049	V_{REF} / 2 + 1 LSB	5.0024V
…	…	…
4095	V_{REF} - 1 LSB	9.9976V

D/A Conversion Formulas for Bipolar Output Ranges

Output voltage = ((D/A code – 2048) / 2048) * Output reference

D/A code = (Output voltage / Output reference) * 2048 + 2048

Example: Output range in bipolar mode = ±10V
Full-scale range = 10V – (-10V) = 20V
Desired output voltage = 2.000V
D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

For the bipolar output range ±10V, 1 LSB = 1/4096 * 20V, or 4.88mV.

Here is an illustration of the relationship between D/A code and output voltage for a bipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for ±10V range
0	$-V_{REF}$	-10.0000V
1	$-V_{REF}$ + 1 LSB	-9.9951V
…	…	…
2047	-1 LSB	-0.0049V
2048	0	0.0000V
2049	+1 LSB	0.0049V
…	…	…
4095	V_{REF} - 1 LSB	9.9951V

10.8 Generating an Analog Output

This chapter describes the steps involved in generating an analog output (also called performing a D/A conversion) on a selected output channel using direct programming (not with the driver software).

There are three steps involved in performing a D/A conversion:

1. **Compute the D/A code for the desired output voltage**
2. **Write the value to the selected output channel**
3. **Wait for the D/A to update**

10.8.1 COMPUTE THE D/A CODE FOR THE DESIRED OUTPUT VOLTAGE

Use the formulas on the preceding page to compute the D/A code required to generate the desired voltage.

Þ **Note:** The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore the maximum possible output voltage is always 1 LSB less than the full-scale reference voltage.

10.8.2 WRITE THE VALUE TO THE SELECTED OUTPUT CHANNEL REGISTERS

First use the following formulas to compute the LSB and MSB values:

LSB = D/A Code & 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example:

Output code = 1776

LSB = 1776 & 255 = 240 (F0 Hex); MSB = int(1776 / 256) = int(6.9375) = 6

The LSB is an 8-bit number in the range 0-255. The MSB is a 4-bit number in the range 0-15.

The MSB is always rounded DOWN. The truncated portion is accounted for by the LSB.

Now write these values to the output registers. The LSB is written to Page 0: Base + 6. The MSB is written to Page 0: Base + 7.

outp(Base + 6, LSB);

outp(Base + 7, MSB);

10.8.3 SET REGISTERS FOR CHANNEL

Now that the value for the given channel is set, the channel selection needs to be made in order to latch the data to the D/A. At this time, the decision must be made as to whether to pass the data to the D/A immediately (“Transparent pass-through” mode) or to latch and hold the data until all of the D/A channels are set (“Simultaneous Update” mode).

“Transparent Mode” will send the data (just written in the previous step) to the D/A beginning immediately after the channel selection is made. The D/A output will be updated as soon as the data is transferred and the internal analog circuitry with a worst-case settling time of ~10usec (as per the DAC7715 specification).

"Simultaneous Update Mode" will latch the data into an internal buffer for that channel, but will not update the A/D until instructed to do so. In this manner, several (or all 4) of the A/D channels can be configured and then updated simultaneously. This allows for a uniform transition time for all A/D outputs.

To send the data to the D/A immediately, write the channel number to Page 0: Base+5 bits 1-0. For Transparent mode, bit 8 should be set to "0":

outp(Base + 5, Channel Number);

Where "Channel Number" is 0-3

To latch the data in preparation for more updates (not sending the data to the D/A until channel data updates are completed), write the channel number to Page 0: Base+5 bits 1-0, with bit 8 should be set to "1". :

outp(Base + 5, 0x80 + Channel Number);

Where "Channel Number" is 0-3

The D/A data will be held until a "0" is written to the Simultaneous Update bit, at which time all of the latched data will be updated at the same time. So, if data has previously been latched with the simultaneous update bit set to "1" and the data for the last channel involved in the simultaneous update has just been written to Base + 6 and Base + 7, then the final channel selection (which would send all of the latched data to the D/A) would look just like a "Transparent Mode" write, i.e.:

outp(Base + 5, Channel Number);

Where "Channel Number" is 0-3

At this point, all of the latched data would be enabled through the D/A and the analog outputs would begin the transition to the selected values at the same time.

10.8.4 WAIT FOR THE D/A TO UPDATE

Writing the channel number to Base + 5, regardless of the state of the "SU" bit, starts the D/A update process for the selected channel(s). The update process requires approximately 30 microseconds to transmit the data to the D/A chip (and then update the D/A circuit in the chip, if the data is to be passed through immediately). During this period, no attempt should be made to write to any other channel in the D/A through addresses Base + 6 or Base + 7.

The status bit DABUSY (Page 0 : Base + 4 bit 5) indicates whether the D/A is busy updating (1) or idle (0). After writing to the D/A, monitor this bit until it is zero before proceeding to the next D/A operation.

Note that the time required to transfer data for a channel occurs whether the "Simultaneous Update" bit is set or not: the data is transferred (and the DABUSY signal is active) regardless of whether the data is to be immediately updated or is being latched in preparation for later simultaneous update. The only difference in the two modes occurs after the Digital data is transferred: in "Transparent mode" the data will immediately pass through the D/A whereas "Simultaneous Update" mode will conclude with the D/A output data unchanged.

10.9 Analog Circuit Calibration Resources

For a board with the Data Acquisition option, the Hercules-EBX Data Acquisition circuitry incorporates some advanced calibration features to allow the system to calibrate both the A/D and D/A signal conversion pathways. The registers involved in controlling these calibration features are listed below:

Register Bit Name	Register location	Signal Name	Description
ADBU	<All pages>Base+1:Bit 0	ADCUNI(OUT)	a one sets A/D section to unipolar input mode
DABU	<All pages>Base+1:Bit 2	DACUNI(OUT)	a one sets D/A section to bipolar output mode
CMUXEN	Page 0:Base+30:Bit 4	MUXEN4(OUT)	a one enables calibration voltages multiplexer
SEDIFF	<All pages>Base+1:Bit 1	ADDIFF(OUT)	a one sets A/D section to differential mode
TrimDAC Data	Page 1 : Base+28 (8-bit)	TrimDAC Data[D7-D0]	Data Sent to TrimDAC
TrimDAC Address	Page 1 : Base+29 : Bits 2-0	TrimDAC Address [A2-A0]	Address for TrimDAC
TDACEN	Page 1 : Base+30 : Bit 3	TDACEN	TrimDAC Enable (when "1") – note that this is mutually-exclusive with EE_EN control

Table 35: Calibration Control Signal Listing

AUTO CALIBRATION TABLE:

When Register bit CMUXEN=1, the board is in auto calibration mode. When this mode is enabled, specific calibration voltages will be fed back to analog channel inputs. There are 5 calibration settings that can be used (named "VCAL0 – 5" below). These feedback voltages are selected based on the "ADCH0" and "ADCH1" settings (ADCH4-2 are ignored during autocalibration):

CMUXEN	SEDIFF	ADCH(1/0)	VCAL	VOLTAGE
0	**Normal Operation**			
1	0	0 (0/0)	0	0
1	0	1(0/1)	1	2.5mV
1	0	2 (1/0)	2	1.12V
1	0	3 (1/1)	3	4.78V
1	1	X	4	VOUT0

Table 36: Calibration Multiplexed Signal Control

Notes:

- VCAL0 is for bipolar A/D offset adjustments
- VCAL1 is for unipolar offset adjustments
- VCAL2 is for full scale 0-1.25, 0-2.5, +/-1.25 and +/-2.5 modes
- VCAL3 is for full scale 0-5, 0-10, +/-5 and +/-10 modes
- VCAL4 is D/A VOUT0 for D/A calibration; this loops Analog output "VOUT0" back

OUTPUT (TrimDAC Address)	NAME	FUNCTION	POLARITY
O0	ADCOFF coarse	A/D offset, all modes, coarse	The same for bipolar, Inversed for unipolar
O1	ADCOFF fine	A/D offset, fine	The same for bipolar, Inversed for unipolar
O2	ADCFUL coarse	A/D full scale, all modes, coarse	Inversed
O3	ADCFUL fine	A/D full scale, fine	Inversed
O4	DACOFF coarse	D/A offset, coarse	Inversed
O5	DACOFF fine	D/A offset, fine	Inversed
O6	DACFUL coarse	D/A full scale, coarse	The same
O7	DACFUL fine	D/A full scale, fine	The same

Table 37: Trim-DAC (AD8801) Outputs

Notes:

- "The same" means: increase in the trimDAC value increases readout and vice versa
- "Inversed" means: increase in the trimDAC value decreases readout and vice versa
- "Coarse" adjustment is the basic trimDAC variance, while "Fine" only affects adjustment of about 1% of full effect in all modes

10.10 Analog Circuit Calibration Procedures

Calibration applies only to boards with the analog I/O circuitry.

The analog I/O circuit is calibrated during production test prior to shipment. Over time the circuit may drift slightly. If calibration is desired, internal autocalibration can be performed using the software routines provided with the Diamond Software driver libraries (part of the Hercules-EBX development kit). For analog I/O circuit configuration see page 63.

Six adjustments are possible:

- A/D bipolar offset
- A/D unipolar offset
- A/D full-scale
- D/A bipolar offset
- D/A unipolar offset
- D/A full-scale

The specific algorithms required to perform autocalibration can be quite involved, and are too detailed to go into at great length here. Suffice it to say that such procedures are provided in the included drivers and that details of autocalibration can be provided as necessary.

Note that the Autocalibration settings are stored in nonvolatile memory in the calibration EEPROM and are reloaded each time the on-board FPGA (or system) is reset.

10.11 Using EEPROM

There is an EEPROM used to store all TrimDAC adjustment values. These values are loaded on reset or power-up, so it is critical that these values be correct in order to maintain accurate A/D measurements. These settings are configured to defaults during manufacturing test – be sure that you know what you are doing before changing these settings.

The EEPROM provides 256 bytes of non-volatile storage. The first 128 (addresses 00-0x7F) bytes are reserved for Auto Calibration settings and should not be overwritten. The last 128 bytes are available for user-accessible non-volatile storage.

Note that access to EEPROM data can be handled through the DSCUD software utilities.

Remember that bytes 0-127 are reserved for system use (TrimDAC autocal values); altering those values will adversely affect system calibration.

10.11.1 READING VALUE FROM EEPROM

Example : read one byte from EEPROM location 128:

```
outp(base+0, 0x01);     // set page to page 1
outp(base+15, 0xA5);    // unlock EEPROM
outp(base+29,0x80);     // set address location to 128 (0x80)
outp(base+30, 0xC0);    // Initiate transfer, set to read
while (inp(base+30) & 0x20);    // Wait for EEPROM load to complete
Data = inpb(base+28);   // data returned from EEPROM access
outp(base+0, 0x00);     // set page to page 0 (and re-enables lock on EEPROM / TrimDAC)
```

10.11.2 WRITING VALUE TO EEPROM

Example : write one byte (value = 0xaa) to EEPROM location 254, then verify the data:

```
outp(base+0, 0x01);     // set page to page 1
outp(base+15, 0xA5);    // unlock EEPROM
outp(base+29,0xFE);     // set address location to 254 (0xFE)
outp(base+28, 0xAA);    // Set data to write to EEPROM
outp(base+30, 0x80);    // Initiate transfer, set to write
while (inp(base+30) & 0x20);    // Wait for EEPROM write to complete
outp(base+15, 0xA5);    // unlock EEPROM
outp(base +29,0xFE);    // set address location to 254 (0xFE)
outp(base+30, 0xC0);    // Initiate transfer, set to read
while (inp(base+30) & 0x20);    // Wait for EEPROM load to complete
Data = inpb(base+28);   // data returned from EEPROM access; data should be 0xAA
outp(base+0, 0x00);     // set page to page 0 (and re-enables lock on EEPROM / TrimDAC)
```

10.12 Digital I/O Operation

Hercules-EBX contains 40 digital I/O lines organized as four 8-bit I/O ports, A, B, C, D, and E. The direction for each port is independently programmable. The ports are accessed at registers Base + 16 through Base + 20 respectively, and the direction register is at Base + 22 (all on Page 0).

Offset	7	6	5	4	3	2	1	0
12	LED	SINGLE	DIOCTR1	DIOCTR0	SCINT	CLKSRC1	CLKFRQ1	CLKFRQ 0
..								
16	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0
17	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0
18	DIOC7	DIOC6	DIOC5	DIOC4	DIOC3	DIOC2	DIOC1	DIOC0
19	DIOD7	DIOD6	DIOD5	DIOD4	DIOD3	DIOD2	DIOD1	DIOD0
20	DIOE7	DIOE6	DIOE5	DIOE4	DIOE3	DIOE2	DIOE1	DIOE0
..								
22	MODE	P2	P1	P0 / DIRE	B2 / DIRD	B1 / DIRC	B0 / DIRB	D / DIRA

Table 38: DIO Data and Control Registers (Page 0)

The digital I/O lines are located at pins 1 through 40 on the I/O header J8 (see page 16). They are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state. See the specifications on page 106 for more detail.

DIRA, DIRB, DIRC, DIRD, and DIRE control the direction of ports A, B, C, D, and E, respectively. A 0 means output and a 1 means input. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

There are two methods of programming the Digital I/O ports: as individual bits (useful for output only) or as bytes (for either input or output).

BIT Mode : To program a specific output bit, bit-mode operation can be used. This is mode is selected by writing a “1” to the MODE bit of the “Digital I/O Configuration / Bit Programming Register” located at Base + 22. When setting this in bit mode, bits 6-4 select the DIO port (A-E, values 0-4), bits 3-1 select the bit within the port (bit selection 0-7), and bit 0 selects the value for the bit in question.

In this mode, an individual output bit for one of the 40 available DIO bits can be individually assigned a value. As an example, the following would set bit 4 of DIO port B to “0” and then would set DIO port B to an output (with all other ports set to input):

```
outp(base+22, 0x98);   // Selects:   Bit Mode (bit 7=1),
                       //            Port B (bits 6-4 = 001),
                       //            bit 4 (bits 3-1 = 100),
                       //            value = 0 (bit 0=0)
outp(base+22, 0x02);   // Selects:   DIO direction Mode (bit 7=0) and
                       //            Port B is output; ports A,C,D,E all inputs
```

BYTE Mode : For byte-mode operation, the data for a given byte is read or written to the appropriate DIO byte register: DIO ports A-E are located at Base+16 – Base+20, respectively. As an example, the following illustrates setting port A to output (B-E to input), writing a value of "AA" to port A, and reading data from port C:

```
outp(base+22, 0x01);   // Selects:   DIO direction Mode (bit 7=0) and
                       //            Port A is output; ports B,C,D,E all inputs
outp(base+16, 0xAA);   // Send data to DIO output port A
data = inp(base+18);   // Read data from port C
```

Note that accessing a Digital Output port can be handled as bit or byte-level accesses interchangeably – the two methods are provided to allow maximum flexibility for output operations.

10.13 Special Digital I/O Operation – Port E

In addition to the standard Digital I/O operation detailed above, port E may alternatively be configured for some special I/O functions, allowing access to several special-purpose Digital I/O controls. These special functions are controlled with the DIOCTR0 and DIOCTR1 bits.

DIOCTR0 controls the special functions for DIO E3-E0:

J8 - Pin Number	DIOCTR0	
	0	1
33	DIO E0	PWM0
34	DIO E1	PWM1
35	DIO E2	PWM2
36	DIO E3	PWM3

Table 39: DIOCTR0 (DIO3-0 Alternate Functions)

See section on PWM functionality for details on PWM functions for these pins (when DIOCTR0 = 1).

DIOCTR1 controls the special functions for DIO E7-E4:

J8 - Pin Number	DIOCTR1	
	0	1
37	DIO E4	GATE 0
38	DIO E5	DIOLATCH
39	DIO E6	TOUT 1
40	DIO E7	GATE 1

Table 40: DIOCTR1 (DIO7-4 Alternate Functions)

See sections on "Counter / Timer Operation" on page 99 and "DIO Handshaking Mode" (below) for details on these special functions (available only when DIOCTR1 is set to "1").

10.13.1 DIO HANDSHAKING OPERATION

Normally, the DIO data is transferred through the data registers with each read. If a handshaking method is desired, two signals are provided to allow this type of transfer:

- DIOLATCH
  - Input to system (low latches all input data; high passes data through directly)
  - Normally pulled-up (passes all DIO data through without handshaking); affected by DIO pull-up's
  - Falling edge generates IRQ when "DINTE" (Base+13, bit 5) is "1"
  - Present on DIO Header J8, pin 39
  - NOTE : Only accessible when "DIOCTR is set to "1"
- ACK
  - Output from system (driven high when DIOLATCH transitions from high-to-low; ACK is driven low as soon as latched data is read into the system)
  - Present on DIO Header J8, pin 43

The handshaking sequence would look similar to this over the course of one data transaction:

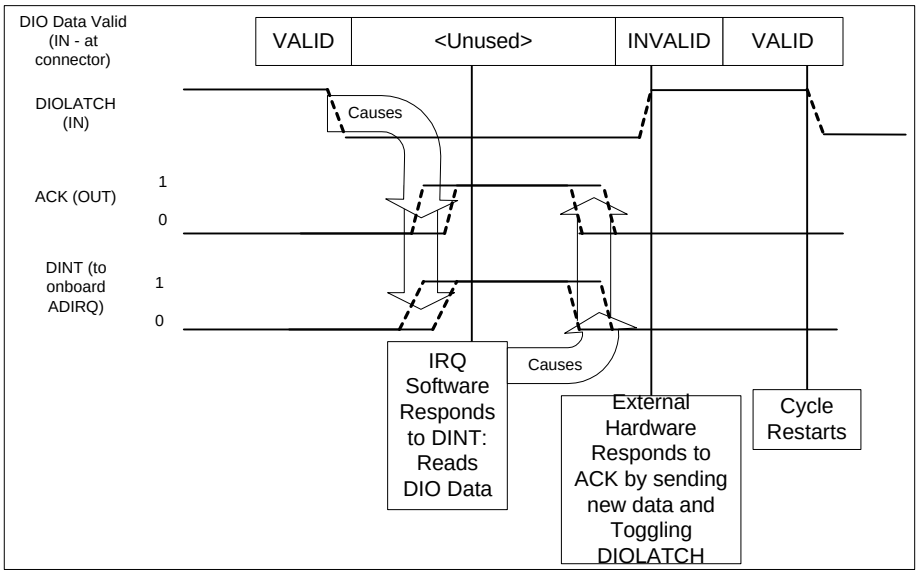


Figure 10 : DIOLATCH / ACK Handshaking Diagram

10.13.2 DIO PULL-UP/DOWN SETTINGS

All DIO signals have some basic ESD and over/under-voltage protection. In addition, all signals can be configured with pull-up or pull-down resistors to set a given I/O voltage when no input signal is provided. This pull-up/pull-down setting should always be made for two reasons:

1. Prevents floating inputs (latch-up from floating input where CMOS I/O pins are involved)
2. Sets a known voltage level for inputs that are not driven

This is particularly useful for signals such as the DIOLATCH and EXTTRIG signals, for example, where a floating input could cause erratic or erroneous results (latch/counter edge trigger could occur randomly).

To set DIO signal pull-ups or pull-downs, a jumper must be added across signals on header J5, as indicated here:

DIO Signal (Range)	Pull-up	Pull-down	Notes
A7-0, B7-0, C7-0, D7-0, E3-0	1-3	3-5	PWM Outputs are included here
E7-4 (GATE0, TOUT1, GATE1, DIOLATCH)	2-4	4-6	Affects DIO Hanshaking and GATE for both Counters

Table 41: DIO Pull-Up/Down Configuration

Note that:

- "Pull-up" means that a weak (47kOhm) pull-up resistor will be connected between the DIO signal and +3.3V. This sets the DIO signal to a "1" value when there is no external source driving the signal.
- "Pull-down" means that a weak (47kOhm) pull-down resistor will be connected between the DIO signal and ground. . This sets the DIO signal to a "0" value when there is no external source driving the signal.
- FPGA programming / updates: These Pull-up/down resistors also affect signal outputs during the period when the FPGA is being loaded or re-loaded. During an FPGA update, the FPGA will briefly tri-state all signals – during this period, the pull-up/down resistors will be the only current source coming from the board through the DIO signals.

So, for example, to set all standard DIO signals to "0" by default and to allow DIO handshaking to be configured such that the DIOLATCH signal is pulled high (for normal handshaking operation default), a jumper would be placed across J5 pins 3-5 (sets normal DIO's to "0" when not driven) and across J5 pins 2-4 (sets DIO E7-E4 to "1" when not driven, including "DIOLATCH" which is present on DIO E6 pin).

11. COUNTER/TIMER OPERATION

Hercules-EBX models with Data Acquisition contain two counter/timers that provide various timing functions on the board for A/D timing and user functions. These counters are controlled with registers in the on-board data acquisition controller FPGA. See pages 67 and 70 for information on the counter/timer control register bits and how to perform various functions using these counters.

11.1 Counter 0 – A/D Sample Control

The first counter, Counter 0, is a 24-bit "divide-by-n" counter used for controlling A/D sampling. The counter has an internal clock input, an external gate input ("Gate 0" – alternate function for DIO Channel E bit 4), and a dedicated output ("TOUT 0"). The input is a 10MHz or 100 kHz clock provided on the board and selected with bit CKFRQ0 in Page 0 Base + 12 bit 0. The gate is an optional signal that can be input on pin 40 of the I/O header J8 when DIOCTR1 (Page 0: Base + 12 bit 5) is 1. If this signal is not used, then the counter runs freely. The "TOUT 0" signal output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output is always present on pin 42 of the I/O header J8.

The counter operates by counting down from the programmed divisor value. When it reaches zero, it outputs a positive-going pulse equal to one input clock period (100ns or 10µs, depending on the input clock selected by CKFRQ0). It then reloads to the initial load value and repeats the process indefinitely.

The output frequency can range from 5MHz (10MHz clock, divisor = 2) down to 0.006Hz (100 kHz clock divided by 16,777,215, or 2^{24}-1). The output is fed into the A/D timing circuit and can be selected to trigger A/D conversions when AINTE is 1 and CLKSEL is 0 in Base + 13 (bit 1). Using the control registers at Page 0 : Base + 13 and Base + 27, the counter can be loaded, cleared, enabled, and disabled, the optional gate can be enabled and disabled, and the counter value can be latched for reading.

11.2 Counter 1 – Counting/Totalizing Functions

The second counter, Counter 1, is similar to Counter 0 except it is a 16-bit counter. It also has an internal clock input, as well as an external input ("EXTTRIG"), an external gate ("GATE 1"), and an output ("TOUT1"). The gate and output signals are present on the I/O header only when DIOCTR=0. The input may come from either the external trigger signal or the on-board clock generator. When the on-board clock generator is used, the clock frequency is either 10MHz or 100 KHz as determined by control bit CKFRQ1, located at Page 0: Base + 12, bit 1.

The output ("TOUT1") is a positive-going pulse that appears on pin 38 of I/O header J8 (when DIOCTR1 = 1). The output pulse occurs when the counter reaches zero. When the counter reaches zero it will reload and start over on the next clock pulse. The output stays high the entire time the counter is at zero, i.e. from the input pulse that causes the counter to reach zero until the input pulse that causes the counter to reload.

When CLKSRC1=1 (external source), then Counter 1 operates as follows: It counts positive edges of the signal on pin 41 ("EXTTRIG") on the I/O header. The counter can either be free running or gated, as determined by the Gate Enable control bit, "GTEN" (Page 0 : Base +27, bit 4).

The gate signal is provided on pin 37 when DIOCTR1 = 1 (enabling counter functions on I/O header) and GTEN = 1 (enabling gating for this counter). If the gate signal is high then the counter will count, and if it is low the counter will hold its value and ignore input pulses. This pin can have a pull-up so the counter can operate without any external gate signal (See section on DIO pull-up's on page 97).

NOTE: When counting external pulses, Counter 1 will only update its read register every 4th pulse. This behavior is due to the synchronous design of the counter having to contend with the asynchronous input pulses. The count register contents are correct on the 4th pulse but will remain static until 4 more pulses occur on the input.

When DIOCTR1=0, Counter 1 operates as follows: It takes its input from the on-board clock generator based on the value of the CKFRQ1 bit located at Page 0: Base + 12. There is no gating and the counter runs continuously.

Counter 1 may be used as either a pulse generator or a totalizer/counter. In pulse generator mode the output signal on pin 26 is of interest. In totalizer/counter mode the counter value is of interest and may be read by first latching the value and then reading it.

11.3 Command Sequences

Diamond Systems provides driver software to control the counter/timers on Hercules-EBX. The information here is intended as a guide for programmers writing their own code in place of the driver and also to give a better understanding of the counter/timer operation.

The counter control register is shown below for reference (from PAGE 0).

Base + 27 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTR	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

To make a counter run (load and enable a counter)

1. Load the desired initial value into the counter.
2. If you want to use the gate function, enable the gate.
3. Enable the counter.

To read a counter

1. Latch the counter. The counter continues to operate.
2. Read the value from the data registers.

A counter may be enabled or disabled at any time. If disabled, the counter will ignore incoming clock edges.

The gating may be enabled or disabled at any time. When gating is disabled, the counter will count all incoming edges. When gating is enabled, if the gate is high the counter will count all incoming edges, and if the gate is low the counter will ignore incoming clock edges.

Loading and enabling a counter

For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer.

a. Write the data to the counter:

Break the load value into 3 bytes, low, middle, and high (two bytes for counter 1). Then write the bytes to the data registers in any sequence.

Counter 0
```
outp(base+24,low);
outp(base+25,middle);
outp(base+26,high);
```

Counter 1
```
outp(base+24,low);
outp(base+25,high);
```

b. Load the counter:

Counter 0
```
outp(base+27,0x02);
```

Counter 1
```
outp(base+27,0x82);
```

c. Enable the gate if desired:

Counter 0
```
outp(base+27,0x10);
```

Counter 1
```
outp(base+27,0x90);
```

d. Enable the counter:

Counter 0	**Counter 1**
outp(base+27,0x04);	outp(base+27,0x84);

Reading a counter

a. Latch the counter:

Counter 0	**Counter 1**
outp(base+27,0x40);	outp(base+27,0xC0);

b. Read the data:

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1)

Counter 0	**Counter 1**

low=inp(base+24);
middle=inp(base+25);
high=inp(base+25);
	low=inp(base+24);
	high=inp(base+25);

c. Assemble the bytes into the complete counter value:

Counter 0	**Counter 1**
val = high * 2^16 + middle * 2^8 + low;	val = high * 2^8 + low;

Enabling the counter gate

Counter 0	**Counter 1**
outp(base+27,0x10);	outp(base+27,0x90);

The counter will run only when the gate input is high.

Disabling the counter gate

Counter 0	**Counter 1**
outp(base+27,0x20);	outp(base+27,0xA0);

The counter will run continuously.

Clearing a counter

Clearing a counter is done when you want to restart an operation. Normally you only clear a counter after you have stopped (disabled) and read the counter. If you clear a counter while it is still enabled, it will continue to count incoming pulses, so its value may not stay at zero.

a. Stop (disable) the counter:

Counter 0	**Counter 1**
outp(base+27,0x08);	outp(base+27,0x88);

b. Read the data (optional). See “Reading a counter” above.

c. Clear the counter:

Counter 0	**Counter 1**
outp(base+27,0x01);	outp(base+27,0x81);

12. PULSE-WIDTH MODULATION OPERATION

Hercules-EBX models that include Data Acquisition contain four PWM generators for automatic generation of a regular pulse with independently-configurable duty cycle and frequency. These output signals are present on DIO Header J8 pins 33-36 (PWM output channel 0-3) when DIOCTR0 = 1.

Each PWM consists of two 24-bit down counters, CT0 and CT1. CT0 controls the frequency, and CT1 controls the duty cycle, or length of the active pulse. Each counter is initially loaded with the desired data, and desired clock frequencies are selected for each counter. CLK1 and CLK0 select 10MHz (0) or 100 KHz (1) for the clock source for their respective counters.

Each counter contains a 24-bit load register. The load registers are accessed by writing to Page 1 base + 24 to base + 26 followed by a load command (base + 27 bit 7 = 0 indicates a PWM command) and may be written to at any time. When ENAB = 0, each counter is loaded from the load register via the load command. When ENAB = 1, each counter is loaded from its load register on the next clock after CT0 = 0.

When ENAB=1, both counters count down at the same time. While CT1 is running, the PWM output is equal to the polarity selected by POL: 1 = the output is high during the active period when CT1 is counting down, and 0 = the output is low during the active period. This causes the output pulse to occur at the start of the cycle.

After CT1 reaches 0, it stops counting, and the output switches to the opposite inactive polarity on the next clock. CT0 runs continuously. When it is 0, on the next clock, both counters will reload from their load registers, and the cycle will repeat.

CT0 and CT1 may be reloaded while the PWM is running. The reload data is held in a separate load register for each counter and is not loaded into the counter until CT0 = 0. This allows the current cycle to complete without distortion. Note that this implies that a long PWM cycle duration for the current cycle may cause a considerable update delay before the new settings are seen on the PWM outputs: if the current PWM cycle period is several seconds in duration and the PWM data is updated near the beginning of a cycle, then the output will not be updated with the new settings until several seconds later.

ENAB controls the operation of the PWM. ENAB = 1 causes the PWM to run, and ENAB = 0 disables the PWM circuit. In the disabled state the PWM retains its current state but does not count input clocks, and the output is set to the inactive state as determined by POL.

OUTEN controls the output signal. If OUTEN = 1 then the output is active, and if OUTEN = 0, the output is equal to the inactive state determined by POL. When POL = 0, the inactive state is 0, and when POL = 1 the inactive state is 1. The truth table is as follows:

CT1 output	POL	OUTEN	Output pin	Comments
0	0	0	1	Active low, active, disabled
0	0	1	0	Active low, active, enabled
0	1	0	0	Active high, inactive, disabled
0	1	1	0	Active high, inactive, enabled
1	0	0	1	Active low, inactive, disabled
1	0	1	1	Active low, inactive, enabled
1	1	0	0	Active high, active, disabled
1	1	1	1	Active high, active, enabled

Table 42: PWM Control Signal Truth Table

12.1 Pulse-Width Modulation Example

The following is a programming example to output a 1KHz signal with a 25% high duty cycle on PWM output 2:

a) Note that, for 1KHz output, either reference clock (10MHz or 100KHz) is suitable. For this example we are going to use the 10MHz reference clock.

b) The first step is to determine the value for the output frequency counter (counter 0)

Counter 0 Value = Reference Clock / Desired Rate

Counter 0 Value = 10MHz / 1Khz

Counter 0 Value = 10000

c) The next step is to determine the value for the duty cycle counter (counter 1).

Counter 1 Value = Timer 0 Value * Duty Cycle

Counter 1 value = 10000 * 0.25

Counter 1 value = 2500

d) Program the two counters:

outp(base + 0, 1); //Set page 1 (for PWM functions)

c0 = Counter 0 Value = 10000

outp(base + 24, (c0 >> 0) & 0xFF); //Counter 0 bits 0-7

outp(base + 25, (c0 >> 8) & 0xFF); //Counter 0 bits 8-15

outp(base + 26, (c0 >> 16) & 0xFF); //Counter 0 bitrs 16-23

outp(base + 27, 0x20); //This loads the value into counter 0 for PWM circuit 2

c1 = Counter 1 Value = 2500

outp(base + 24, (c1 >> 0) & 0xFF); //Counter 1 bits 0-7

outp(base + 25, (c1 >> 8) & 0xFF); //Counter 1 bits 8-15

outp(base + 26, (c1 >> 16) & 0xFF); //Counter 1 bitrs 16-23

outp(base + 27, 0x21); //This loads the value into counter 1 for PWM circuit 2

e) Configure and enable PWM output 2. These are the desired configuration values for base+27:

BIT7 = 1;	Indicates PWM configuration byte
PWM0-1 = 2;	Program PWM output 2
CLK = 0;	Use the 10MHz reference clock

POL = 1;	Active state = high (PWM will be high for the 25% duty cycle)
OUTEN = 1;	Enable PWM output
ENAB = 1;	Enable PWM circuit

From these settings we get a configuration byte of 0xA7 (see page 73 for register description.)

outp(base + 0, 1); //Set page 1 (for PWM functions)

outp(base + 27, 0xA7); //Configure and enable PWM output 2

f) Finally, to enable PWM outputs (replacing Digital I/O Port E, bit3-0 : see page 96), set DIOCTR0 = 1, leaving the rest of the Configuration Register as-is:

Data = inp(base + 12); // Read current Configuration Register settings

Data = Data || 0x10; // Set DIOCTR0 = 1, forcing PWM3-0 onto DIO

outp(base + 12, Data); // Write settings back to Configuration Register

At this point, a 1KHz signal with a 25% high duty cycle will be present on PWM output 2 (J8 – pin 35).

13. WATCHDOG TIMER PROGRAMMING

13.1 Example : Watchdog Timer With Software Trigger

Software trigger relies on a thread of execution to constantly trigger watchdog timer A. If the thread is ever halted, timer A will reach zero and start timer B. Once timer B reaches 0, the board will reset.

In this example we will set the watchdog timer to a countdown period of 4 seconds. Note that longer timeout periods should typically be used when relying on software-based triggers for the Watchdog Timer in order to accommodate varying software latencies (Interrupt latencies, other tasks with priority at certain times, etc)

Setting up the watchdog timer:

outp(base + 0, 0x00);	//set page 0
outp(base + 28, 40000 & 0xFF);	//set LSB of WD timer A (4 seconds)
outp(base + 29, (40000 >> 8) & 0xFF);	//set MSB of WD timer A
outp(base + 30, 0xFF);	//set WD timer B to 0.0255 seconds
outp(base + 31, 0x28);	//set WDEN=1, WDRST=1 (enable WD timer, reset)

The timer is now setup and active. A separate thread should now be constantly running this code:

```
while (1)
{
  outp(base + 31, 0x80);        //trigger watchdog timer
  sleep(1000);                  //sleep one second
}
```

If this thread is interrupted or if the parent process crashes, then the board will reset 4 seconds after the last trigger is received.

13.2 Example : Watchdog Timer With Hardware Trigger

Hardware trigger relies on an external pulse to constantly trigger watchdog timer A. If the external stream of pulses is ever halted, timer A will reach zero and start timer B. Once timer B reaches 0, the board will reset.

In this example, we will make use of the "T-1" feature of timer A to automatically reset itself unless a physical connection is broken. The physical connection must be made between WDO and WDI on the data acquisition header J9.

Since software is not involved in maintaining the timer, we do can set the reset period to a much smaller value. In this example, the reset pulse will travel across the physical connection every 10 milliseconds.

```
outp(base + 0, 0x00);                 //set page 0
outp(base + 28, 100 & 0xFF);          //set LSB of WD timer A (10 milliseconds)
outp(base + 29, 100 >> 8) & 0xFF);    //set MSB of WD timer A
outp(base + 30, 0xFF);                //set WD timer B to 0.0255 seconds
outp(base + 31, 0x2D);                //set WDEN=1, WDRST=1, WDT-1=1, WDIEN=1
```

Now when timer A reaches 1, a rising edge will flow from WDO to WDI, resetting the timer back to 100 and lowering WDO. When the connection from WDO to WDI is severed, the rising edge will never reach WDI and system will reset.

14. DATA ACQUISITION SPECIFICATIONS

These specifications apply to units with Data Acquisition Only

Analog Inputs

No. of inputs	16 differential or 32 single-ended (user selectable)
A/D resolution	16 bits (1/65,536 of full scale)
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1.25V Unipolar: 0-10V, 0-5V, 0-2.5V
Input bias current	50nA max
Maximum input voltage	±10V for linear operation
Overvoltage protection	±35V on any analog input without damage
Nonlinearity	±3LSB, no missing codes
Drift	5PPM/^{o}C typical
Conversion rate	100,000 samples per second max
Conversion trigger	software trigger, internal pacer clock, or external TTL signal
FIFO	48 samples; programmable interrupt threshold

Analog Outputs

No. of outputs	4
D/A resolution	12 bits (1/4096 of full scale)
Output ranges	Unipolar: 0-10V or user-programmable Bipolar: ±10V or user-programmable
Output current	±5mA max per channel
Settling time	4µS max to ±1/2 LSB
Relative accuracy	±1 LSB
Nonlinearity	±1 LSB, monotonic

Digital I/O

No. of lines	40 (32 dedicated DIO plus two configurable nibbles, 4-bits each)
Compatibility	3.3V and 5V logic compatible
Input voltage	Logic 0: -0.5V min, 0.8V max; Logic 1: 2.0V min, 5.5V max
Input current	±1µA max
Output voltage	Logic 0: 0.0V min, 0.4V max; Logic 1: 2.4V min, 3.3V max
Output current	Logic 0: 12mA max; Logic 1: -8mA max
I/O capacitance	10pF max

Counter/Timers

A/D pacer clock	24-bit down counter with optional external gate
Pacer clock source	10MHz, 100 kHz, or external signal
General purpose	16-bit down counter with optional external gate
GP clock source	10MHz, 100 KHz, or external signal

General

Power supply	+5VDC ±5%
Current consumption	0.7A – 1.1A typical
Operating temperature	-40 to +85^{o}C
Operating humidity	5% to 95% noncondensing

15. FLASHDISK MODULE

Hercules-EBX is designed to accommodate an optional flashdisk module. This module contains 32MB to 128MB of solid state non-volatile memory that operates like an IDE drive without requiring any additional driver software support.

Model	Capacity
FD-32	32MB
FD-64	64MB
FD-96	96MB
FD-128	128MB

15.1 Installing the Flashdisk Module

The flashdisk module installs directly on the IDE connector J16 and is held down with a spacer and two screws onto a mounting hole on the board.

The flashdisk module contains a jumper for master/slave configuration. For master, install the jumper over pins 1&2, and for slave install the jumper over pins 2&3.

15.2 Configuration

To configure the CPU to work with the Flashdisk module, enter the BIOS (press F2 during startup). Select the Main menu, and then select IDE Primary Master. Enter the following settings:

Type:	User
Cylinders:	489 for 32MB flashdisk
Heads:	4 for 32MB flashdisk
Sectors:	32 for 32MB flashdisk
Multi Sector Transfer:	Disable
LBA Mode Control:	Enable
32 Bit I/O:	Disable
Transfer Mode:	Fast PIO 1
Ultra DMA Mode:	Disable

Exit the BIOS and save your change. The system will now boot and recognize the FlashDisk module as drive C:.

15.3 Using the Flashdisk with Another IDE Drive

Since the flashdisk occupies the board's IDE connector, mounting it on the board prevents the simultaneous use of another IDE drive with the same IDE port. To utilize both the flashdisk and another drive, an adapter board, such as Diamond Systems' ACC-IDEEXT, and cables are required. The ACC-IDEEXT adapter board is described on page 116.

15.4 Power Supply

The 44-pin cable carries power from the CPU to the adapter board and will power the flashdisk module and any drive using a 44-pin connector, such as a notebook hard drive.

A drive utilizing a 40-pin connector, such as a CD-ROM or full-size hard drive, requires an external power source through an additional cable. The power may be provided from the CPU's power out connector (J12) or from one of the two 4-pin headers on the ACC-IDEEXT board.

Diamond Systems' cable no. **698006** may be used with either power connector to bring power to the drive.

16. “UTILITY” BOARD

A small “Utility” board (DSC# **861002**) has been designed for test and development with the Hercules-EBX. It is included with the Hercules-EBX development system (DSC# **DK-HRCEBX-01**). This small board plugs onto the “Utility” connector J7and provides a simple interface for various buttons / LED’s:

- Power Button – simple push-button for “Power Button” functionality
- Reset Button – push button causes systemwide hardware reset
- Power LED – lights when main system power is active (note that stand-by power may still be active when this LED is off)
- Ethernet : 100MBit link LED – lights up when 100Mbit link is achieved (will not be illuminated for 10Mbit link)
- Ethernet : Activity LED – pulses with Ethernet activity (reads or writes)
- IDE Activity LED : Lights when any access is made through the two onboard IDE connectors (reflects activity of up to 4 devices potentially active through the two IDE connectors)
- Speaker – this speaker is a typical PC “Beep” speaker; it is not an output for the onboard sound system at all

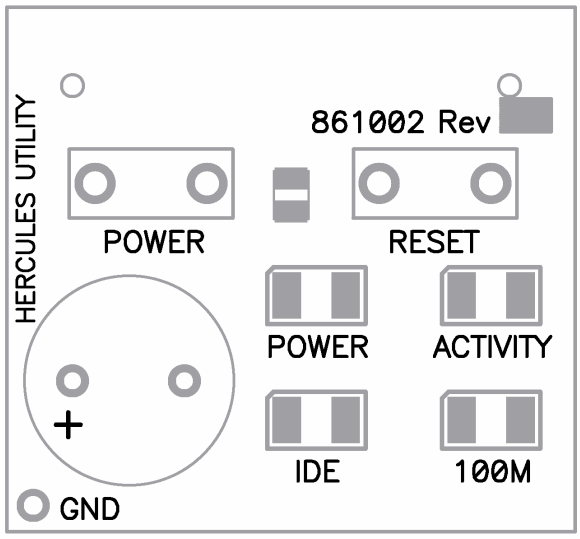


Figure 11 : Utility Board (for J7)

17. DATA ACQUISITION TEST BOARD

The Data Acquisition Test Board (DSC# **ACC-HRCDAQ**) is provided with the Hercules-EBX development system as a means to do simple tests and verification of the onboard Data Acquisition system (both digital and analog I/O).

The DAQ test board consists of two connectors for ribbon cables (one for digital I/O, the other for analog I/O), A sequence of LEDs (for visual display of one byte of DIO loopback), a bank of DIP switches, and 3 sets of test points.

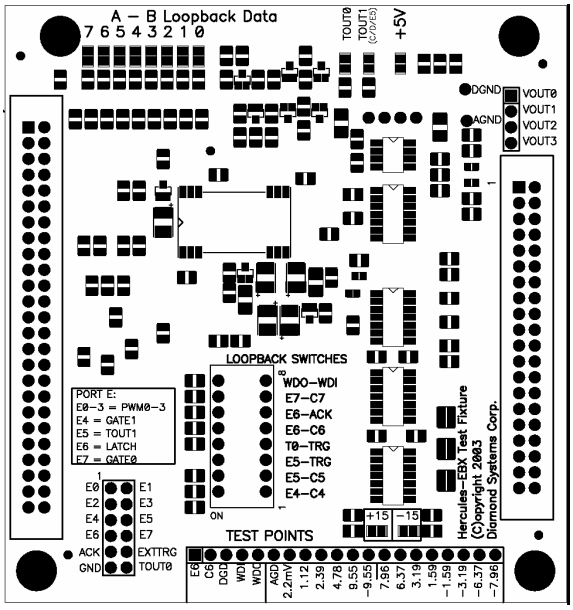


Figure 12 : Data Acquisition (DAQ) Test Board

17.1 Connecting the DAQ Test Board

The DAQ Test board is powered from the ribbon cables and contains sensitive analog amplifiers wired to these cables. As such, the board should only be connected or disconnected while the Hercules-EBX power is "OFF" (standby power is OK – main power, as indicated by the "ON" LED on the main board, should be off).

- One 50-pin ribbon cable (DSC part # **C-50-18**) should be connected from the Hercules-EBX board connector J8 to the DAQ test board J3. Note the pin "1" designations on both boards – ensure that the ribbon cable is connected such that the red pin-1 designation on the ribbon cable is oriented next to the "1" on the board silk screen for each board.
- One 40-pin ribbon cable (DSC part # **C-40-18**) should be connected from the Hercules-EBX board connector J9 to the DAQ test board J2. Note the pin "1" designations on both boards – ensure that the ribbon cable is connected such that the red pin-1 designation on the ribbon cable is oriented next to the "1" on the board silk screen for each board.
- Before using the board, make certain that all DIP switches (SW1 bank) are not conflicting – the best way to ensure this is to set all DIP switches to the "OFF" position.
- Apply power to the main board (press "Power Button" on utility board if main board has been powered off using the on-board power control) and watch for the "+5", "+15", and "-15" LEDs to become active.
- At this point, the board should be ready-to use.

17.2 DAQ Board DIO interface

The Data Acquisition Test Board provides a complete loopback capability for each DIO bit: each DIO signal can potentially be driven and read back by at least one other DIO channel. The details of this loopback are user-configurable for many DIO bits – see details below.

17.2.1 DIO A – DIO B LOOPBACK

DIO channel A (bits 7-0) are looped back to DIO channel B (bits 7-0). There is one special case for this loopback: bit 0 also goes to "EXTTRIG".

In general, this loopback requires that one port be set up as an output and the other port should be set as an input (on the Hercules-EBX, via software). While there is some protection for the case of both set as outputs, this should not be done and serves no useful purpose in testing.

This loopback is connected to a bank of 8 LED's on the test board. A given LED will be active when the associated data bit is low. For example, if DIO channel A is set as an output and DIO channel B is set as an input then a value of "0xFE" written to the DIO Channel A output register would result in "0xFE" in the channel B input register and would result in one LED (bit 0) being "ON" while the rest of the DIO loopback LED's would be off.

To perform DIO loopback tests, ensure that one of the channels is set as an output and the other channel is set as an input. Any data written to the output channel should be read back on the input channel.

17.2.2 DIO C – DIO D – DIOE LOOPBACK

DIO channel C (bits 7-0) is looped back to DIO channel D (bits 7-0) and DIO channel E (bits 7-0) (through some switches for bits 7-4). For basic loopback testing, switch bank SW1 would be set such that:

- Switch 1 is ON (E bit 4 connected to C bit 4 and D bit 4)
- Switch 2 is ON (E bit 5 connected to C bit 5 and D bit 5)
- Switch 3 is ON (E bit 6 connected to C bit 6 and D bit 6)
- Switch 4 is OFF (E bit 6 NOT connected to ACK output)
- Switch 5 is ON (E bit 7 connected to C bit 7 and D bit 7)

(NOTE: Switch 6 does not affect DIO loopback – it is for watchdog timer functions)

To perform DIO loopback tests, ensure that one of the three channels is set as an output and the other two channels are set as inputs. Any data written to the output channel should be read back on the two input channels.

There are several special cases for Channel E testing:

- Channel E, bits 3-0 can also be used for the Pulse-Width Modulation output function. In this case, channels C and D would both need to be configured as inputs to avoid out-output contention. These PWM waveforms can be readily sampled via DIO Channel C 3-0 or DIO Channel D 3-0, or they can be manually measured at pins 1-4 on testpoint connector TP1.
- Channel E, bit 4 can also be used for the "GATE1" function. It can be connected to DIO Channel C and D bit 4 by selecting SW1 – switch 1 to the "ON" position. In this configuration, it is directly wired for DIO loop back to Channel C bit 4 and Channel D bit 4.

  To test "GATE1" functionality, one of the other sources must be set as an output to assert the required signal or SW1 – switch 1 can be set to the "OFF" position and an

appropriate signal can be driven into test point TP1 – pin 4. This test point can be used for “GATE1” probing and assertion.

- Channel E, bit 5 is wired to an LED on-board, as well as to SW1 – switch 2. To loopback DIO E bit 5 to DIO C/D bit 5, set SW1-switch 2 to the “ON” position. To test “TOUT1” functionality for DIO E – bit 5, either set both DIO D and C to input or set SW1 – switch 2 to the “OFF” position. DIO E bit 5 can be manually measured at TP1 – pin 6.
- Channel E, bit 6 (which is also used for “LATCH” signal functionality) can be independently connected to DIO channel C / D bit 6 (for DIO loopback testing) or the “ACK” output signal (for “LATCH” functional testing). Test point TP1 – pin 7 can be used for “DIO E bit 6 / LATCH” probing and assertion.
    i. For loopback testing, SW1 – switch 3 should be set “ON” and SW1-switch 4 should be set “OFF”.
    ii. For LATCH / ACK testing, SW1 – switch 4 should be set “ON” and SW1-switch 3 should be set “OFF”.
- Channel E, bit 7 can also be used for the “GATE0” function. It can be connected to DIO Channel C and D bit 4 by selecting SW1 – switch 5 to the “ON” position. In this configuration, it is directly wired for DIO loop back to Channel C bit 7 and Channel D bit 7. Test point TP1 – pin 8 can be used for “GATE0” probing and assertion.

In general, DIO loop back requires that one port be set up as an output and the other two ports should be set as an input. While there is some protection for the case of two or more outputs, this should not be done and serves no useful purpose in testing.

17.2.3 SPECIAL FUNCTIONS

As has been mentioned previously, Channel E can be used for alternative functions for the DIO interface. In addition, there are several dedicated signals for some of these special functions. (See the section 95 for more details).

- GATE 0 – This signal is used to enable the internal counter 0 of the FPGA, when in “gated mode”. A high input enables counting and a low input disables counting. This signal is multiplexed with Channel E bit 7, which means that this input is tied directly to Channel D bit 7 and channel C bit 7 when SW1 – switch 5 is “ON”. To test this special function input, either one of these DIO channels (C or D) must be set as an output and bit 7 of the output channel must be used to control this gating function.

  Alternatively, an external source can be used. In this case, SW1 – switch 5 should be set to “OFF” and an external gating signal should be driven in to TP1 – pin 8.

- GATE 1 - This signal is used to enable the internal counter 1 of the FPGA, when in “gated mode”. A high input enables counting and a low input disables counting. This signal is multiplexed with Channel E bit 4, which means that this input is tied directly to Channel D bit 4 and channel C bit 4 when SW1 – switch 1 is “ON”. To test this special function input, either one of these DIO channels (C or D) must be set as an output and bit 4 of the output channel must be used to control this gating function.

  Alternatively, an external source can be used. In this case, SW1 – switch 1 should be set to “OFF” and an external gating signal should be driven in to TP1 – pin 5.

- TOUT0 – This signal is used as a timer out from the FPGA timer 0 control. It is a dedicated output, and is tied to an LED and a test point (TP1 – pin 12) for probing.

- TOUT1 - This signal is used as a timer out from the FPGA timer 1 control. It is multiplexed with Channel E bit 5, and is wired directly to Channel D bit 5 and

Channel C bit 5 as well as to an LED. If "TOUT1" function is required, then the two attached DIO signals (D bit 5 and C bit 5) must be configured as inputs. "TOUT1" is also tied to a test point (TP1-pin6) for probing.

- DIOLATCH / ACK – The "LATCH" signal is multiplexed with DIO Channel E Bit 6. The output is connected directly to the dedicated "ACK" signal via SW1-switch 4, so DIO feedback can be directly supported for testing. If this is selected, SW1-switch 3 should be set "OFF" to avoid conflicts (DIO C/D bit 6 unintentionally driving DIOLATCH).

- EXTTRIG – This is a dedicated input signal which is used for latching data or as a clock or pulse source for the internal counter 1. This is connected directly to a test point (TP1-pin 10), Channel A bit 0, Channel B bit 0, as well as two switches :

  i. SW1-switch 3 which routes EXTTRIG to DIO E5 / TOUT1

  ii. SW1-switch 4 which routes EXTTRIG to TOUT0

  There are several ways to test EXTTRIG, given these connections:

  i. Use TOUT0 to drive EXTTRIG. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "ON", DIO ports A and B should both be configured as INPUT, and TOUT0 should be configured to generate the desired output.

  ii. Use TOUT1 to drive EXTTRIG. In this case, SW1-switch 3 should be "ON", SW1-switch 4 should be "OFF", DIO ports A and B should both be configured as INPUT, and TOUT1 should be configured to generate the desired output (making sure that DIO Channel E7-4 are configured for alternate functions).

  iii. Use DIO A bit 0 to drive EXTTRIG. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "OFF", DIO port B should both be configured as INPUT, and DIO port A should be configured as OUTPUT. Data written to DIO port A, bit 0 would then control the EXTTRIG function.

  iv. Use DIO B bit 0 to drive EXTTRIG. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "OFF", DIO port A should both be configured as INPUT, and DIO port B should be configured as OUTPUT. Data written to DIO port B, bit 0 would then control the EXTTRIG function.

  v. Use external trigger source. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "OFF", DIO ports A and B should both be configured as INPUT, and DIO port B should be configured as OUTPUT. The external trigger source should be connected via TP1-pin 10.

- Pulse-Width Modulation Output – There are 4 channels of PWM output that can be independently controlled. These four channels are present on Channel E bits 3-0 when the PWM functions are enabled. Frequency and duty cycle can be varied for each channel.

NOTE: Be certain that the DIP switches for the DIOLATCH / ACK handshaking are correctly configured on the DAQ Test Board before beginning any testing of these functions. If a DIO is inadvertently connected to this lookback, anomalous behavior may result. As mentioned above for LATCH / ACK testing, SW1 – switch 4 should be set "ON" and SW1-switch 3 should be set "OFF".

17.3 DAQ Board Analog Testing

17.3.1 ANALOG OUTPUT CONNECTIONS

There are 4 output channels (VOUT3-0) from the main Hercules board. All of these are capable of full-rail (+/- 10V) output, and are looped back to input channels for testing. These connections are like so:

- VOUT 0 -> VIN9 and VIN 12 (both buffered); Also, is inverted to VIN10
- VOUT 1 -> VIN13
- VOUT 2 -> VIN14
- VOUT 3 -> VIN15

17.3.2 ANALOG INPUT CONNECTIONS

There are 32 single-ended analog input channels (or 16 differential input channels). These channels are configured like so:

- VIN 0 = Ground (0 V)
- VIN 1 = “Vlowref” (2.2mV)
- VIN 2 = “+Vref-L” (1.1161V)
- VIN 3 = (2.39V)
- VIN 4 = “+Vref-H” (4.7768V)
- VIN 5 = “V+” (9.5536V)
- VIN 6 = “V-“ (-9.5536V)
- VIN 7 = Ground (0 V)
- VIN 8 = Ground (0 V)
- VIN 9 = VOUT 0 (buffered)
- VIN 10 = -VOUT 0 (buffered)
- VIN 11 = Ground (0 V)
- VIN 12 = VOUT 0 (buffered)
- VIN 13 = VOUT 1
- VIN 14 = VOUT 2
- VIN 15 = VOUT 3
- VIN 16 = Ground (0 V)
- VIN 17 = Ground (0 V)
- VIN 18 = Ground (0 V)
- VIN 19 = Ground (0 V)
- VIN 20 = Ground (0 V)
- VIN 21 = Ground (0 V)
- VIN 22 = Ground (0 V)
- VIN 23 = “V-“ (-9.5536V)
- VIN 24 = (7.961V)
- VIN 25 = (6.369V)
- VIN 26 = (3.185V)
- VIN 27 = (1.592V)
- VIN 28 = (-1.592V)
- VIN 29 = (-3.185V)
- VIN 30 = (-6.369V)
- VIN 31 = (-7.961V)

17.3.3 GENERAL DAQ TESTING SUGGESTIONS / COMMENTS

- Differential Bipolar / Unipolar settings: Note the differential pairs in the listing above. Specifically, note that VIN5+ would be connected to +9.5V and VIN5- would be ground; VIN6+ would be -9.5V and VIN6- would be ground. If the A/D inputs are configured for differential mode and all voltages look correct up to VIN6 (i.e., VIN0-3 look correct, you get a reading of +9.5V for VIN5, but VIN6 is reading 0V), this is a good indication that the inputs are configured for unipolar mode (i.e., negative differential voltage not being reported). Similarly, voltage readings for channels VIN8

and VIN11 would also be incorrect and readings for VIN9, VIN10, VIN12, VIN13, VIN14, and VIN15 may not be correct (depending on whether the output voltage is higher than the associated “low-side” differential voltage for the given input channel).

- Due to the cable length and relative board location, some of the outputs may show more noise / inaccuracy than others. This board is intended as a means to verify basic functionality and connection (including autocalibration features); it is not intended to provide perfect response for signal performance characterization.

18. FLASH DISK PROGRAMMER BOARD

The Flash Disk Programmer Board accessory model no. **ACC-IDEEXT** may be used for several purposes. Its primary purpose is to enable the simultaneous connection of both a flashdisk module and a standard IDE hard drive or CD-ROM drive to allow file transfers to/from the flashdisk. This operation is normally done at system setup. The board can also be used to enable the simultaneous connection of two drives to the CPU.

J1 connects to the IDE connector on Hercules-EBX with a 44-pin ribbon cable (Diamond Systems' part no. **698004**). Both 40-pin .1" spacing (J4) and 44-pin 2mm spacing (J3) headers are provided for the external hard drive or CD-ROM drive. A dedicated connector (J2) is provided for the flashdisk module. Any two devices may be connected simultaneously using this board with proper master / slave jumper configurations on the devices.

The Flash Disk Programmer Board comes with a 44-wire cable no. (DSC no. **698004**) and a 40-wire cable no. (DSC no. **C-40-18**) for connection to external drives. The flashdisk module is sold separately.

The 44-pin connector (J1, J2, and J3) and mating cable carry power, but the 40-pin connector (J4) and mating cable do not. J5 and J6 on the accessory board may be used to provide power to a 44-pin device attached to the board when the board is attached to a PC via a 40-pin cable. These headers are compatible with the floppy drive power connector on a standard PC internal power cable.

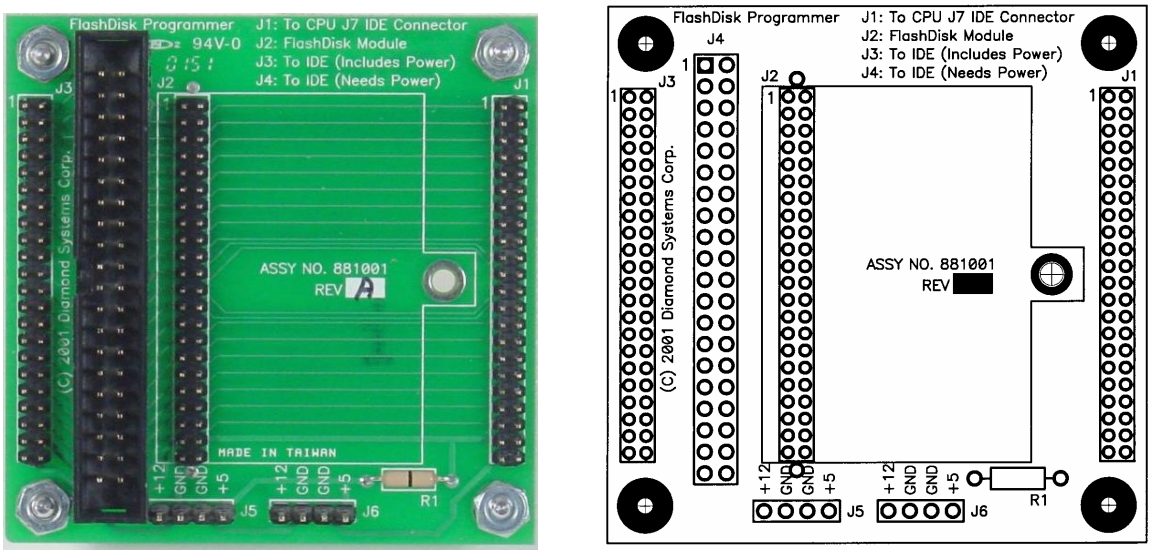


Figure 13 : ACC-IDEEXT *FlashDisk Programmer Board*

19. I/O CABLES

For custom installations as well as development, Diamond Systems offers a cable kit no. **<DSC# C-HRCEBX-KIT>** with 18 types of cables to connect to all I/O headers on the board. Some cables are also available separately.

The mating cable for each I/O connector is listed in Chapter 4.

NOTE: When the multi-I/O cable (DSC# **C-DB9M-4**) or any other cable is connected to serial ports 1,2,3 or 4, the serial port signals must terminate to another board, or interference problems may occur that will slow down the performance of your CPU.

Photo No.	Cable No.	Description
1	**C-PRZ-02**	(OPTIONAL) 6-wire Ethernet cable with panel-mount RJ-45 connector
2	**698022**	PS/2 Connector for Mouse and Keyboard with PS/2 mini-DIN connectors
3	**698025**	Audio I/O Cable (for line-level and microphone audio)
4	**698017**	TV out cable (S-Video mini-DIN and Composite RCA jack output) NTSC-only
5	**698018**	Amplified audio output (Speaker out), with volume control signals with stripped/tinned leads
6	**698024**	VGA Ribbon cable to VGA Female DB15 for monitor out
7	**C-20-18**	18-inch ribbon cable for “Utility” connections (includes power and reset contacts)
8	**C-40-18**	40-wire data acquisition ribbon cable (Analog I/O)
9	**C-50-18**	50-wire data acquisition ribbon cable (Digital I/O)
10	**C-DB9M-4**	40-pin ribbon cable to 4-serial port male DE-9 connectors
11	**698026**	UDMA/ATA-100 cable for 1 or 2 IDE drives
12	**698004**	44-wire IDE cable for 1 or 2 laptop-style drives
13	**698015**	Standard (low-voltage) input power cable with stripped/tinned leads for connection to external power source
14	**698016**	(OPTIONAL) High-Voltage DC power input cable
15	**698001**	External (3V) Battery power cable
16	**698006**	4-wire output power cable for external drives
17	**698012**	Dual USB cable
18	**861002**	Utility Board (used instead of **C-20-18** for development)

Table 43: Hercules-EBX Cable Kit (DSC#C-HRCEBX-KIT)

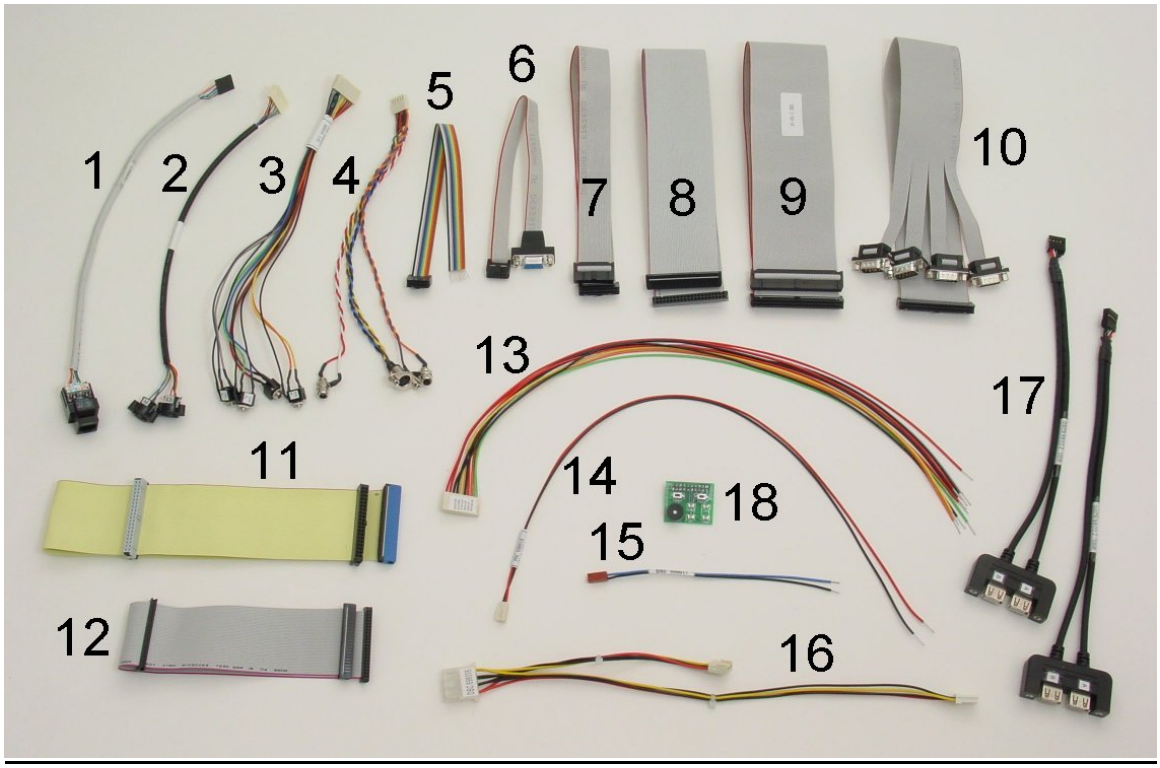


Figure 14 : Hercules-EBX Cable Kit

20. MOUNTING PC/104(+) CARDS ONTO A HERCULES-EBX BASEBOARD

Hercules-EBX is designed to serve as a baseboard for a stack of PC/104 or PC/104+ boards. Up to 4 PC/104+ boards are supported with the top-most board only supporting slave-mode PCI – no bus mastering supported for that board. Any PC/104 boards should be mounted on top of the PC/104+ board stack, when both board types are to be combined (this should be obvious, given the lack of PC/104+ stack-through connectors on a standard PC/104 board).

PC/104+ requires a board configuration setting for each board in a PC/104+ board stack. Ensure that the lowest board in the stack is assigned to lowest board ID, as per the PC/104+ specification. This setting establishes the PCI Clock, PCI Interrupt routing, the Bus Master signals, and the device ID setting for PCI configuration. Note that these settings are critical – two boards should never be configured with identical board stack settings, as this will cause problems accessing PCI devices, and may cause damage to the main board and/or the PC/104+ boards in the stack. **Do not configure two PC/104+ boards with the same board stack ID!**

PC/104 is much less critical in this regard, but care should be taken to ensure that the ISA resource allocations allow space for the specific boards added in the stack. Resources (IRQ's in particular) can be very limited in a system with so many devices present on the main board. It is important to ensure that ISA I/O, Memory, IRQ, and DMA configuration conflicts are resolved before powering the system up. Otherwise, it is possible that the system boot sequence might be impeded by such conflicts.

Take care to read through this documentation (the section on ISA Resource defaults, in particular) to familiarize yourself with the internal resources used before adding components that might cause conflicts.

When adding boards to the PC/104(+) board stack, be sure to include board standoffs. Inordinate flexing of the main PC/104 and PC/104+ connectors can seriously reduce the effective lifespan of the connectors, as well as causing potential system instability due to incomplete connection across system buses.

21. COMPACT FLASH

There is a Compact Flash connector located on the bottom of the board, under J34. A Compact Flash card placed in this slot will be recognized as an IDE device and will be treated as such. A Compact Flash card can be used as the boot device for a system Note that Compact Flash installation requires that no cable connections be made to J17 – no other IDE devices are supported in this channel when a Compact Flash card is installed (the Primary IDE channel would still be available).

Note that the board is not configured for CompactFlash support by default. To enable CompactFlash, add a jumper to J5 (to enable MASTER support). With this jumper added, any card placed in the CompactFlash slot should be detected as an IDE device upon boot-up. See jumper detail on page 35.

NOTE: Do not add or remove a CompactFlash card while the board is powered-up. Either remove power from the entire system or power the board off before making these changes.

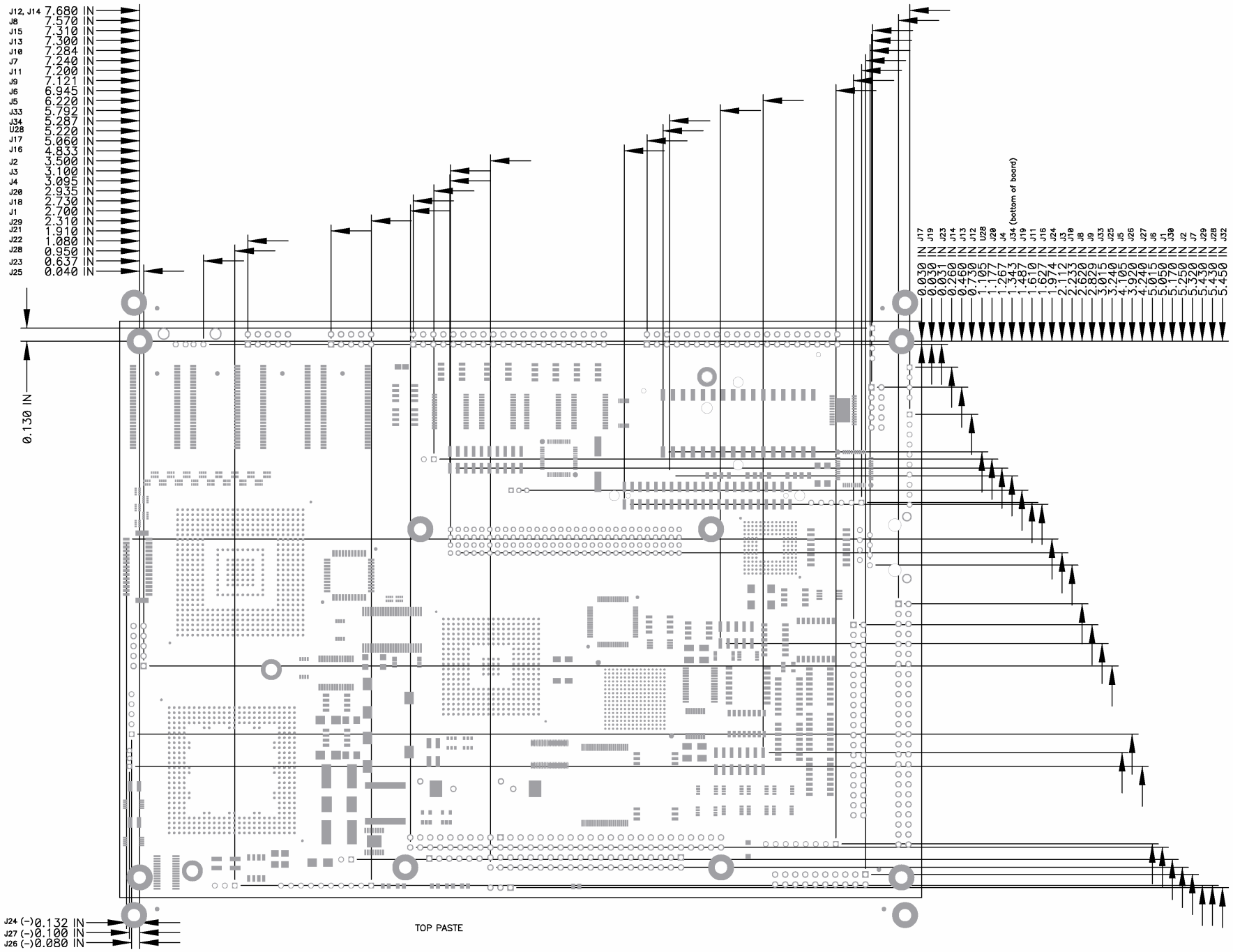
22. CUSTOMIZATION OPTIONS

There are many customer-specific customizations that can be done for the Hercules-EBX, including:

- Latching connectors (replacing the box headers used for most of the board I/O connections)
- Connectors with extra gold contact plating

- Alternative heatsinks for low air-flow and dusty environments
- Conformal Coating
- Jumperless configuration (all settings made on-board with no jumper headers required)

See your sales representative for details on these special-order options.


J12, J14 7.680 IN
J8 7.570 IN
J15 7.310 IN
J13 7.300 IN
J10 7.284 IN
J7 7.240 IN
J11 7.200 IN
J9 7.121 IN
J6 6.945 IN
J5 6.220 IN
J33 5.792 IN
J34 5.287 IN
U28 5.220 IN
J17 5.060 IN
J16 4.833 IN
J2 3.500 IN
J3 3.100 IN
J4 3.095 IN
J20 2.935 IN
J18 2.730 IN
J1 2.700 IN
J29 2.310 IN
J21 1.910 IN
J22 1.080 IN
J28 0.950 IN
J23 0.637 IN
J25 0.040 IN
0.130 IN
J17 0.030 IN
J19 0.030 IN
J23 0.031 IN
J14 0.260 IN
J15 0.460 IN
J13 0.730 IN
U28 1.105 IN
J20 1.177 IN
J4 1.267 IN
J34 (bottom of board) 1.343 IN
J19 1.467 IN
J11 1.610 IN
J16 1.627 IN
J24 1.974 IN
J3 2.112 IN
J10 2.233 IN
J8 2.620 IN
J9 2.829 IN
J33 3.015 IN
J25 3.240 IN
J5 4.105 IN
J26 3.920 IN
J27 4.240 IN
J6 5.015 IN
J1 5.050 IN
J30 5.170 IN
J2 5.250 IN
J7 5.320 IN
J29 5.430 IN
J28 5.430 IN
J32 5.450 IN
J24 (–) 0.132 IN
J27 (–) 0.100 IN
J26 (–) 0.080 IN
TOP PASTE
TOP SOLDER MASK

The following drawing is from the PC/104 specification. This document may be downloaded from www.pc104.org or from www.diamondsystems.com/support/techliterature.

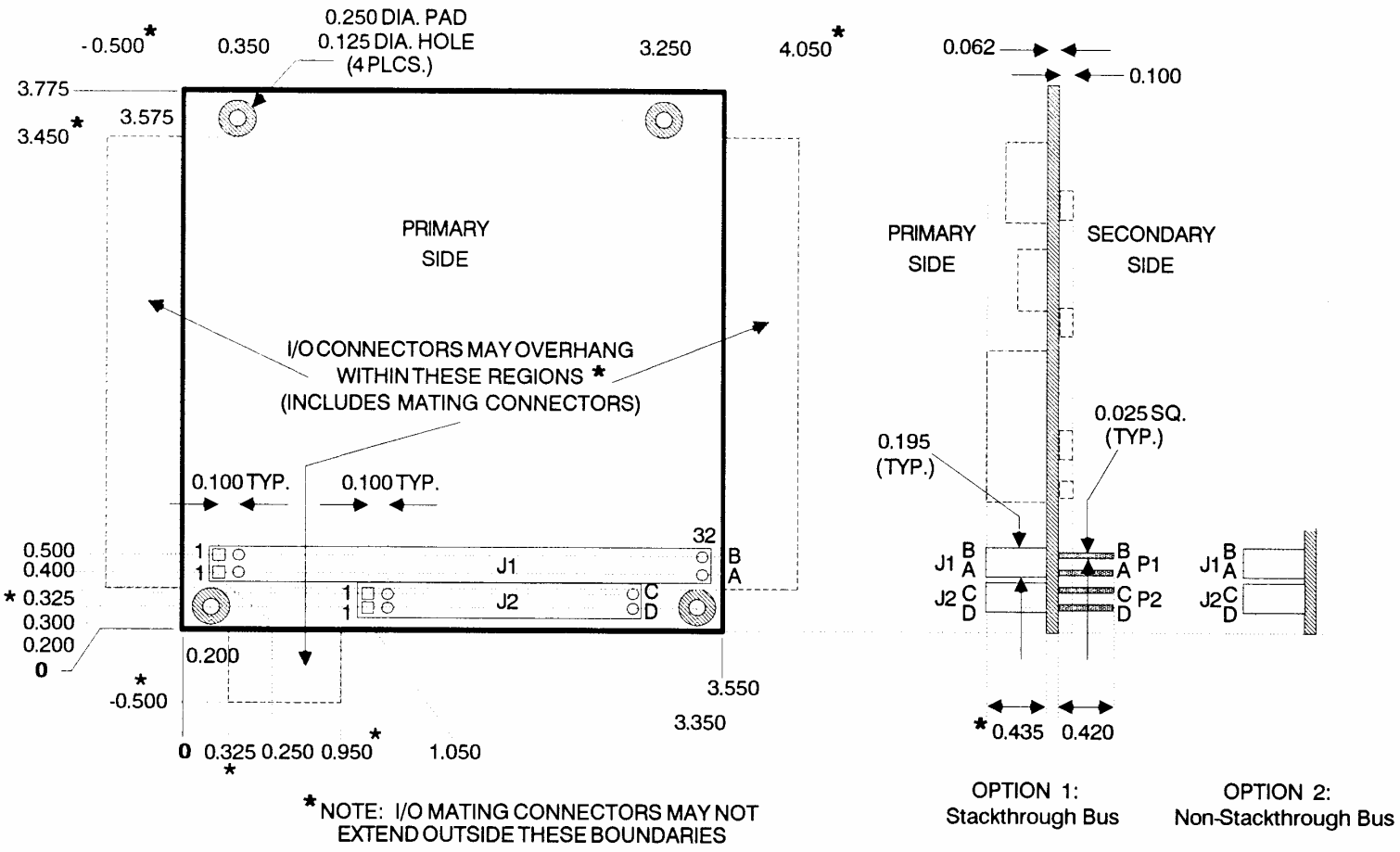


Figure 4: Module Dimensions